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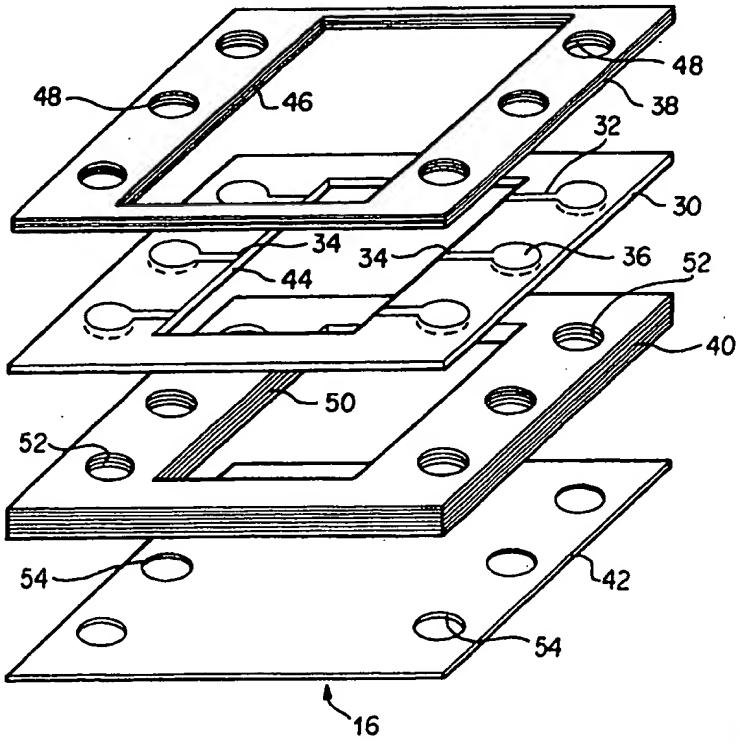
(54) Title: CHIP STACK AND METHOD OF MAKING SAME

(57) Abstract

A stackable chip carrier, made from plural layers of Kapton or other plastic material, and which may be made using conventional flex circuit techniques, has a central opening, a plurality of stacking apertures extending through the thickness thereof between opposite surfaces of the carrier and a conductive pattern therein which extends between the central opening and the stacking apertures. A chip is mounted within the central opening, and is electrically coupled to the conductive pattern such as by wire bonding or by soldering a ball grid array or other arrangement of contacts on the chip directly to the conductive pattern, and is encapsulated therein with potting compound using conventional chip–on–board encapsulation technology, to form a single layer integrated circuit element. Conductive elements such as metallic balls are inserted into the stacking apertures, and are mounted therein using solder or conductive epoxy, so as to electrically contact the conductive pattern and form a stackable IC chip package. A stack of the chip packages is assembled by arranging a stack of the packages so that the metallic balls which protrude from a surface of each package are inserted into the stacking apertures of an adjacent chip package, where they are electrically and mechanically secured by solder or conductive epoxy. Balls mounted within the stacking apertures of a lowermost one of the chip packages protrude from the bottom surface thereof, so that the completed chip stack forms a ball grid array product.



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CHIP STACK AND METHOD OF MAKING SAME

Background Of The Invention

1. Field Of The Invention

The present invention relates to chip stacks in which a plurality of integrated circuit chip packages arranged in a stack are electrically connected in a desired fashion and to methods of making such stacks.

2. History Of The Prior Art

Various common approaches are used to increase memory capacity on a circuit board. Larger memory IC chips can be used, if available. The size of the circuit board can be increased in order to hold more IC chips. Vertical plug-in boards can be used to increase the height of the mother board. The memory devices can be stacked in pancake style (sometimes referred to as 3D packaging or Z-Stacking). The Z-Stacking approach interconnects from 2 to as many as 8 chips in a single component which can be mounted on the "footprint" of a single package device. This approach is the most volumetrically efficient. Package chips in TSOP (thin small outline package) or LCC (leadless chip carrier) form have been used for stacking, and are perhaps the easiest to use. Bare chips or dies have also been used, but the process for forming a stack thereof tends to be complex and not well adapted to automation.

In forming a stack of IC chips such as memory chips, the chips must be formed into a stack and at the same time must be electrically interconnected in desired fashion. Typically, the chips, which are mounted within packages therefor, have most of the electrical contacts thereof coupled in common or in parallel to contacts on a supporting substrate, and several unique contacts which are coupled individually to the substrate to the exclusion of the other chips. The prior art includes various different arrangements for electrically interconnecting the IC chips in a stack. For example, electrical conductors which may comprise thin film metal on an insulating base may be disposed perpendicular

to the planes of the planar chips so as to connect those conductors on each chip which are exposed through openings in an insulating layer. Where the chip packages are assembled into a stack, electrical connections may be accomplished by lead frames or solder strips extending along the sides of the stack and attached to the electrical contacts of the chips.

Another common technique for providing the desired electrical interconnections in a chip stack is to form a stack of chips having bonding pads disposed on the chips adjacent the outer edges thereof. After assembling the stack of chips, the chip edges are ground flat and polished before sputtering an insulating layer thereon. The bonding pads on the edges of the chips are masked during the sputtering process to avoid covering them with the insulating layer. Next, a metal layer is sputtered onto the entire edge of the stack in conjunction with photomasking which forms conductor traces of the metal layer in desired locations for connecting the bonding pads.

Further examples of vertical stacks of IC chips and various methods of making such stacks are provided by U.S. Patents 4,956,694, 5,313,096 and 5,612,570, which patents are commonly assigned with the present application. U.S. Patent 5,612,570, which issued March 18, 1997 and is entitled CHIP STACK AND METHOD OF MAKING SAME, describes a chip stack and a method for making the same in which chip packages are first assembled by mounting plastic packaged chips or thin, small outline package chips (TSOPs) within the central apertures of thin, planar frames having a thickness similar to the thickness of the packaged chip. Leads at opposite ends of the package are soldered to conductive pads on the upper surface of the surrounding frame. Each frame also has other conductive pads on the upper and lower surface thereof adjacent the outer edges of the frame, which are coupled to the conductive pads that receive the leads of the packaged chip by conductive traces and vias. A chip stack is then formed by stacking together a plurality of the chip packages and dipping the outer edges of the stack into molten solder to solder together the conductive pads adjacent the outer edges of the frames. The conductive pads adjacent the outer edges of the frame can be interconnected in a stair step arrangement, and pads on opposite sides of each frame can be coupled in offset fashion using vias, in order to achieve desired electrical

interconnections of the various chips.

A still further example is provided by copending application Serial No. 08/935,216, filed September 22, 1997 and entitled CHIP STACK AND METHOD OF MAKING SAME. Such application, which is commonly assigned with the present application, describes formation of a stack of ball grid array chip packages by assembling a ribbon-like structure of thin, planar bases, each with plural terminals and an interconnecting conductive pattern thereon, and with the bases electrically interconnected by flex circuits extending therebetween. A different chip package is mounted on each base by soldering the balls of a ball grid array thereon to the terminals of the base. The bases alternate in orientation, so that alternate chip packages are joined to the tops and bottoms of the bases. The resulting arrangement is then folded over on itself, with chip packages being joined to adjacent bases using adhesive. The resulting chip stack is mounted on a substrate by soldering the balls of the ball grid array at the underside of the lowermost base at the bottom of the stack to the substrate. The conductive patterns on the bases and the interconnecting flex circuits form conductive pads which contact selected terminals of the various chip packages as the paths extend in alternating fashion through the chip stack between opposite sides of the stack.

A still further example is provided by copending application Serial No. 08/971,499, filed November 17, 1997 and entitled METHOD OF MAKING CHIP STACKS. Such application, which is commonly assigned with the present application, describes the making of a chip stack which begins with the formation of a plurality of panels having apertures therein and conductive pads on opposite sides thereof. Solder paste is deposited on the conductive pads prior to mounting plastic packaged IC chips within each of the apertures in each of the panels so that opposite leads thereof reside on the conductive pads as opposite sides of the apertures. The plural panels are then assembled into a stack, such as by use of a tooling jig which aligns the various panels and holds them together in compressed fashion. The assembled panel stack is heated so that the solder paste solders the leads of the packaged chips to the conductive pads and interfacing conductive pads of adjacent panels together, to form a panel stack comprised

of a plurality of chip package stacks. Following cleaning of the panel stack to remove solder flux residue, the individual chip package stacks are separated from the panel stack by cutting and breaking the stack. Score lines across the topmost panel and transverse slots within remaining panels therebelow result in the formation of strips of chip package stacks when longitudinal cuts are made through the panel stack. The remaining portions of the uppermost panel within such strips are then snapped along the score lines thereof to separate the individual chip package stacks from the strips.

The various arrangements and methods described in the patents and patent applications noted above have been found to provide chip stacks and methods which are advantageous and which are suited for many applications. Nevertheless, the provision of further alternative arrangements and methods would be advantageous. In particular, it would be advantageous to provide chip stacks and methods of making such stacks which utilize available materials and known process techniques. The assembly of such stacks should lend itself to automated production methods, and thus would be competitive with other stacking approaches.

Brief Summary Of The Invention

The foregoing objects and features are achieved in accordance with the invention by a chip stack and methods of making the same which use available materials and known process techniques and in which automated production methods can be used. A thin stackable chip carrier is preferably made from plastic material such as Kapton, using conventional flex circuit techniques to assemble a plurality of different layers to form the chip carrier. A chip is mounted within a central opening in the carrier, and is electrically coupled to a conductive pattern within the carrier, before being encapsulated with a potting compound using conventional chip-on-board encapsulation technology. The chip carrier is formed with a plurality of stacking apertures or pockets which extend through the thickness thereof between opposite surfaces and which receive portions of the conductive pattern within the chip package. Electrical interconnections are accomplished by mounting spherical balls or other conductive elements within the apertures so as to

electrically contact the portions of the conductive pattern within the apertures. The balls protrude from the surfaces of the chip carrier, thereby facilitating insertion of such balls within the apertures of adjacent chip carriers when forming a stack. The stack is thus formed using ball grid array technology, and the resulting stack has balls protruding from the bottom surface of the lowermost chip carrier, so that the stack forms a ball grid array component.

In preferred embodiments according to the invention, the stackable chip carrier includes a base layer with a conductive pattern on at least one surface thereof, a top layer mounted on the base layer and having a central aperture therein, and a center layer mounted on the base layer opposite the top layer and having a central opening therein. A plurality of stacking apertures or pockets extend through the entire thickness of the chip carrier defined by the base, top and center layers. The top and center layers, and a portion of the base layer other than the conductive pattern, are preferably made of Kapton or other plastic material using conventional flex circuit technology, enabling the stackable chip carrier to be made very thin without warpage or other undesirable effects. For certain applications, a bottom layer is mounted on the center layer opposite the base layer and has apertures therein aligned with the plurality of stacking apertures. The conductive pattern may be provided by layers of copper cladding on opposite sides of the base layer which are etched to form a desired conductive pattern.

With metallic balls mounted within the stacking apertures in the chip carrier, desired electrical interconnections of the balls with the conductive pattern are achieved by appropriately configuring the conductive pattern within the stacking apertures. Thus, the base layer can be provided with an aperture within the stacking aperture which is plated through between the layers of copper cladding. Alternatively, the base layer may be without an aperture therethrough in the stacking aperture, so as to have the layers of copper cladding on the opposite sides thereof. Also, the base layer may have an aperture therein adjacent the stacking aperture, which aperture is plated through between the layers of copper cladding. Still further, the base layer may have an aperture therein within the stacking aperture, but with one and not the other of the layers of copper cladding

extending through the aperture in the base layer. In a still further connective arrangement, a portion of one of the layers of copper cladding is extended between an adjacent pair of the stacking apertures, and the base and center layers are provided with apertures therethrough adjacent the portion of one of the layers of copper cladding, so that a tool can be inserted through the apertures in the base and center layers to sever the portion of one of the layers of copper cladding if desired.

The stackable chip carrier is formed into a single layer integrated circuit element by installing a chip therein. The chip is mounted within the central opening in the carrier and is electrically connected to the conductive pattern within the carrier. In the case of a bare chip which has contacts on the outside thereof, such contacts are wire bonded to adjacent conductive pads forming a part of the conductive pattern. Where the chip has balls protruding from a surface thereof, such as in the case of a chip scale package (CSP) or a ball grid array (BGA), the balls are soldered to a portion of the conductive pattern, which serves to mount the chip within the central opening as well as electrically coupling the chip to the conductive pattern. Following installation and electrical interconnection of the chip, an appropriate encapsulant such as potting compound is introduced into the central opening so as to surround and encapsulate the chip.

In cases where the chip being installed in the chip carrier has contacts which are concentrated at the opposite ends thereof, the conductive pattern within the carrier may be designed so as to present conductive pads at opposite ends of the central opening in the chip carrier. After mounting the chip within the central opening, the conductive pads are wire bonded to the contacts at the opposite ends of the chip. The stacking apertures may be located at the opposite ends of the chip carrier adjacent the conductive pads. In a further arrangement in which the chip has contacts concentrated at the opposite ends thereof, the chip carrier may be formed with a layer adjacent the chip that has openings at opposite ends thereof adjacent the contacts at the opposite ends of the chip and a conductive pattern thereon having pads adjacent the openings in the opposite ends of the layer. The pads are wire bonded to the contacts at the opposite ends of the chip. The stacking apertures may be spaced along opposite sides of the chip carrier between the

openings in the opposite ends of the layer and with the conductive pattern on the layer extending to the stacking apertures.

An IC chip stack is formed using a plurality of the single layer integrated circuit elements. Metallic balls or other conductive elements are mounted within the stacking apertures or pockets so as to protrude from the surfaces of the chip carriers. The balls may be mounted within the stacking apertures using conductive epoxy or solder, so that they make electrical contact with the conductive pattern of the chip carrier. Protrusion of the balls from the surfaces of the chip carrier facilitates insertion of the balls into the stacking apertures of adjacent chip carriers, where the balls are also secured and electrically interconnected using either conductive epoxy or solder. Mounting of the balls between the adjacent chip carriers in this fashion serves to mechanically secure the chip stack together. At the same time, the balls are electrically coupled to the conductive patterns within the chip carriers and form conductive columns extending through the stack. A desired conductive pattern arrangement can be achieved by configuring the conductive pattern within the stacking apertures in the manner previously described.

Brief Description Of The Drawings

A detailed description of the invention will be made with reference to the accompanying drawings. in which:

Fig. 1 is a perspective view of a chip stack in accordance with the invention;

Fig. 2 is a perspective view of the chip stack of Fig. 1, taken from a different angle so as to illustrate the manner in which metal balls protrude from the bottom surface of a lower one of the chip packages within the stack;

Fig. 3 is a cutaway view of the chip stack of Fig. 1;

Fig. 4 is a cross-sectional view of the chip stack of Fig. 1 taken along the line 4-4 thereof;

Fig. 5 is an exploded perspective view of the stackable chip carrier used in the chip packages of the stack of Fig. 1;

Figs. 6A-6E are sectional views of a portion of one of the chip packages of the

stack of Fig. 1 showing different electrical interconnection arrangements which are possible in the stacking apertures of the chip package;

Figs. 7A-7C are broken-away perspective views showing different arrangements of chips mounted within chip carriers in the chip packages of the stack of Fig. 1;

Figs. 8A and 8B are broken-away perspective views of two different arrangements for mounting bare chips within the chip carriers to form the IC chip packages of the chip stack of Fig. 1;

Fig. 9A is a broken-away perspective view and Fig. 9B is an exploded, partly broken- away, perspective view, showing two different arrangements for mounting chips having surface ball contacts in chip carriers to form chip packages in the chip stack of Fig. 1;

Figs. 10A and 10B are cross-sectional views of the arrangements of Fig. 9A and 9B respectively;

Fig. 11 is a sectional view of a two-high stack in which the lower package comprises a transposer board;

Fig. 12A is an exploded perspective view of a chip carrier in which conductive elements comprised of fuzz buttons or wire masses are mounted in the stacking apertures;

Fig. 12B is a sectional view of a two-high stack of chip packages using the chip carrier shown in Fig. 12A;

Fig. 13 is a plan view of an elongated chip with contacts at opposite ends thereof wire bonded to adjacent conductive pads of a conductive pattern which extends to stacking apertures located at opposite ends of the chip carrier;

Figs. 14A and 14B are top and end views of a portion of a chip package in which contacts at the opposite ends of an elongated chip are wire bonded to a conductive pattern which reroutes the connections to stacking apertures arranged along opposite side edges of the chip carrier;

Fig. 15 is a side view of a commercially available ball grid array chip;

Figs. 16A and 16B are top and side views of an arrangement in which the ball contacts of the chip of Fig. 15 are soldered to a conductive pattern which reroutes the

connections to stacking apertures located around the perimeter of the chip carrier;

Fig. 17 is a block diagram of the successive steps in a method of making a stackable chip package in accordance with the invention; and

Fig. 18 is a block diagram of the successive steps in a method of assembling a plurality of chip packages made by the method of Fig. 17 into a chip stack.

Detailed Description

Figs. 1 and 2 show an IC chip stack 10 in accordance with the invention. The chip stack 10 is a two-high stack comprised of two different chip packages 12 and 14. However, it should be understood by those skilled in the art that the chip stack 10 can comprise almost any number of chip packages, with stacks of 4, 6 or even 8 packages being possible.

As described in detail hereafter, each of the chip packages 12 and 14 is principally comprised of a relatively thin, generally planar chip carrier 16, made of combinations of plastic such as Kapton and/or other suitable plastic materials. Each chip carrier 16 mounts an IC chip (not shown in Figs. 1 and 2) therein, so that the chip is in electrical contact with a conductive pattern within the chip carrier 16. After mounting of the chip within the chip carrier 16, potting compound 18 is added to a central opening 20 in the chip carrier 16 to encapsulate the chip and seal it from the outside of the chip carrier 16. The conductive pattern within the chip carrier 16, to which the chip is electrically coupled, extends to each of a plurality of cylindrical apertures 22 which form interconnection pockets on opposite sides of the generally planar chip carrier 16 and in alignment with mating chip carriers to be stacked at the top and bottom thereof. Conductive elements, such as metallic spheres or balls 24, are mounted in the apertures 22 so as to contact the portions of the conductive pattern which extend to the apertures 22. The balls 24, which are mounted in the apertures 22 using conductive epoxy or solder, protrude from a surface of the chip carrier 16. The balls 24, which protrude from the surface of a chip package, are received within the apertures 22 of an adjacent chip package, in which they are mounted and extend into electrical contact with the conductive

pattern of such chip package. The balls 24 provide desired electrical interconnections of the chip packages within the chip stack 10. They also facilitate alignment and mechanical interconnection of the adjacent chip packages and, when mounted within the apertures 22 of both chip packages of an adjacent pair, secure the chip packages together within the chip stack 10. The various balls 24 within the chip stack 10 form conductive columns within the chip stack 10. Within each chip package 12 and 14, the connections of the balls 24 to the conductive pattern can be varied to provide a desired pattern of interconnections between the balls 24 and the chips within the chip packages 12 and 14.

Figs. 3 and 4 show the internal details of the chip packages 12 and 14 of the chip stack 10. A different IC chip 26 is mounted within the central opening 20 of the chip carrier 16 of each of the chip packages 12 and 14, and is sealed therein by the potting compound 18. In the present example, each of the chips 26 is a bare chip which has a plurality of contacts 28 on an upper surface thereof. Each of the chip carriers 16 has a base layer 30 therein with a conductive pattern 32 thereon. As described in detail hereafter, the conductive pattern 32 may extend to opposite sides of the base layer 30, particularly within the apertures 22. The conductive pattern 32 includes a plurality of bonding pads 34 adjacent the chip 26. The bonding pads 34 are electrically coupled to the contacts 28 of the chip 26, such as by wire bonding. Wedge bonding using gold wire is preferred, and provides a low profile. In this manner, the chip 26 is electrically interconnected with the conductive pattern 32 of the chip carrier 16 thereof. The conductive pattern 32, in turn, is electrically interconnected in desired fashion with the balls 24 in the apertures 22.

As shown in Figs. 3 and 4, a plurality of the balls 24 are present at the interface between the chip packages 12 and 14 so as to extend into the apertures 22 in both of the chip packages 12 and 14. The balls 24 are mounted within the apertures 22 using conductive epoxy or solder. This mechanically secures the balls 24 within the apertures 22, to couple together the chip packages 12 and 14 within the chip stack 10. It also ensures that the balls 24 make proper electrical contact with portions of the conductive pattern 32 within the apertures 22. Figs. 3 and 4 depict two different examples of the

manner in which the balls 24 can be electrically coupled to the conductive patterns 32 within the apertures 22.

As shown in the left hand portion of each of Figs. 3 and 4, the base layer 30 of the chip carrier 16 of each chip package 12 and 14 extends through the apertures 22 and has no apertures therein. The conductive pattern 32 is present on both of the opposite surfaces of the base layer 30 within the apertures 22. Consequently, a ball 24 at the underside of a base layer 30 makes electrical contact with the conductive layer at the underside of the base layer 30. Conversely, a ball 24 at the top of the base layer 30 makes electrical contact with the layer of the conductive pattern 32 on the upper surface of the base layer 30. The various conductive layers of the conductive patterns 32 can be routed so as to provide desired interconnections between the balls 24 and the chips 26.

The right hand portions of Figs. 3 and 4 depict a different example of the configuration of the conductive patterns 32 within the apertures 22. In this instance, each of the base layers 30 of the chip carrier 16 within the chip packages 12 and 14 has an aperture 36 therethrough within the aperture 22. Within the apertures 36 in the base layers 30, the conductive pattern 32 is plated through between the upper and lower conductive layers thereof. Such configuration provides a common electrical interconnection between the balls 26 at the upper and lower sides of a base layer 30 and the conductive pattern 32 thereof. These and other variations of the interconnect possibilities within the apertures 22 are described hereafter in connection with Figs. 6A-6E.

Fig. 5 is an exploded perspective view of the various layers which comprise the chip carrier 16. The chip carrier 16 includes the base layer 30, a top layer 38, a center layer 40 and a bottom layer 42. The base layer 30 includes the conductive pattern 32 with the bonding pads 34 adjacent a central opening 44 therein. In the present example, the base layer 30 is comprised of a 3 mil thick sheet of Kapton or other suitable plastic material, each of the opposite surfaces of which has a 1 mil thick layer of adhesive thereon which bonds a different 1 mil thick layer of copper cladding thereto. Etching is used to remove unwanted portions of the copper cladding, so that the desired conductive

pattern 32 remains. The conductive pattern 32 shown in Fig. 5 corresponds to the conductive patterns 32 shown in Figs. 3 and 4. Consequently, the bonding pads 34 on the left side of the base layer 30 form parts of conductive traces which extend to the apertures 22 on the left side of the chip carrier 16. At the apertures 22, the conductive trace on the top surface of the base layer 30 covers portions of the upper surface of the base layer 30 in the region of the apertures 22. Although not shown in Fig. 5, corresponding portions of the opposite lower surface of the base layer 30 are covered with a layer of the copper material. On the right side of the base layer 30, the bonding pads 34 form parts of conductive traces which extend to the apertures 36 in the base layer 30. The conductive copper layer extends around the circumference of the apertures 36 and is plated through to the undersides of the apertures 36.

The top layer 38 comprises a 5 mil thick sheet of Kapton or other suitable plastic material having a central opening 46 therein. The central opening 46 of the top layer 38 is larger than the central opening 44 of the base layer 30, so as to expose the bonding pads 34 of the conductive pattern 32 when the top layer 38 is mounted on the base layer 30. The top layer 38 has apertures 48 at opposite sides thereof which coincide with and form portions of the apertures 22 in the assembled chip carrier 16.

The center layer 40 comprises a 10 mil thick sheet of Kapton or other suitable plastic material having a central opening 50 therein which generally coincides with the central opening 44 in the base layer 30. The center layer 40 also has apertures 52 which align with and form portions of the apertures 22 in the assembled chip carrier 16. The center layer 40 is mounted on the opposite side of the base layer 30 from the top layer 38. The bottom layer 42 is mounted on the opposite side of the center layer 40 from the base layer 30.

The bottom layer 42 is a 2 mil thick sheet of Kapton or other suitable plastic material having apertures 54 at opposite sides thereof. The apertures 54 align with and form portions of the apertures 22 in the assembled chip carrier 16. The central openings 44, 46 and 50 within the base layer 30, the top layer 38 and the center layer 40 respectively, combine to form the central opening 20 within the chip carrier 16.

It will be appreciated that the multi-layer structure of the chip carrier 16 readily lends itself to fabrication using presently known flex circuit technology. Such technology further enables the use of Kapton or other plastic material in the fabrication and assembly of the chip carrier 16. Unlike more conventional ceramic materials used in making chip carriers, which materials tend to warp when made in thin layers, the Kapton or other plastic material of the chip carrier 16 according to the invention can be used to form very thin layers within the chip carrier 16. Consequently, the assembled chip carrier 16 is relatively thin, and has a total width which is not much greater than the chip 26 that is mounted therein. This provides for the manufacture of chip packages of substantial thinness, and the assembly of a chip stack of considerable thinness, even where a relatively large number of chip packages are included in the stack.

Figs. 6A-6E illustrate some of the different interconnections that can be used within the apertures 22. Two such interconnections are shown and described in connection with the left and right sides of the chip stack 10 illustrated in Figs. 3 and 4.

A first type of interconnection shown in Fig 6A corresponds to the interconnections shown at the right hand sides of the chip stack 10 of Figs. 3 and 4. This is a straight through connection in which the upper and lower copper layers of the conductive pattern 32 are electrically coupled by plating through an aperture 36 in the base layer 30. This type of interconnection combines with the balls 24 to provide straight through conductive columns within the chip stack 10. Such interconnections are useful for connecting power, ground, address lines or similar common terminals of the various chips 26.

Fig. 6B shows another type of interconnection which is like the interconnections at the left hand sides of the chip stack 10 of Figs. 3 and 4. In this case, the base layer 30 extends through the aperture 22 in the chip carrier 16 and has no aperture therein. The conductive pattern 32 over the aperture 22 and includes upper and lower layers of the copper cladding, with the lower layer contacting the ball 24 shown in Fig. 6B. This type of interconnection is used when a straight through connection is not required. It is particularly useful for "stair step" connections of the chip terminals, and in the case of the

transposer board described hereafter in connection with Fig. 11.

A third type of interconnection is shown in Fig. 6C. In this case, the base layer 30 extends through the aperture 22 and has no apertures therein within the aperture 22. Instead, the base layer 30 has an aperture 56 therein at a location adjacent but spaced apart from the aperture 22. At the aperture 56, the opposite copper layers of the conductive pattern 32 are plated through so as to electrically interconnect with each other. This type of interconnection is useful in connecting selected portions of the top and bottom copper layers of the conductive pattern 32.

A fourth type of interconnection is shown in Fig. 6D. In this case, the base layer 30 has an aperture 58 therein which coincides with the aperture 22 in the chip carrier 16. The conductive pattern 32 consists of only the upper copper layer extending across the aperture 58 in the base layer 30. The ball 24 extends upwardly and into contact with the single upper copper layer of the conductive pattern 32. This type of interconnection provides an inexpensive approach, and is useful where "stair step" type crossover connections are not required.

Fig. 6E illustrates a fifth type of interconnection which is useful for opening a circuit to program a chip package for a specific position within the chip stack 10. This type of approach eliminates "stair step" interconnections. In the arrangement of Fig. 6E, the base layer 30 extends through both of the apertures 22 illustrated. The only aperture in the base layer 30 is an aperture 60 which is located adjacent to but spaced from one of the apertures 22. The aperture 60 is plated through so as to interconnect upper and lower copper layers on the base layer 30. The lower copper layer extends through both apertures 22 where it contacts each of the balls 24 inserted into the apertures. Separate portions of the upper copper layer reside over the apertures 22. A portion 62 of the lower copper layer extends through an aperture 64 formed within the base layer 30 and the center layer 40 beneath the base layer 30. During configuration of the chip package in preparation for installation as part of the chip stack 10, it may be necessary to sever the portion 62 of the conductive pattern 32. This is accomplished by inserting a tool 66 into the aperture 64 and through the portion 62. The interconnection types illustrated in Figs.

6A-6E are illustrated in conjunction with only the base layer 30 and the center layer 40 of the chip carrier 16, for simplicity of illustration. In actual practice, the top layer 38 is present over the base layer 30. Also, the bottom layer 42 is typically present at the bottom of the center layer 40, but is not used in all instances as described hereafter.

Figs. 7A-7C show three different arrangements for packaging a bare chip or die. In this connection, the term bare chip or die is intended to mean a generally rectangular chip having an arrangement of contacts on the outer surface thereof. If the contacts are generally uniformly spaced around the outer periphery of the chip, so that a chip stack formed therefrom can accommodate 40 mil pitch ball grid spacing, then the arrangement shown in Fig. 7A is preferred. The chip 26 is mounted within the central opening 20 in the chip carrier 16 using adhesive. Wire bonds are made using a gold wire wedge bonder, to interconnect the relatively evenly spaced contacts 28 on the chip 26 with the bonding pads 34 spaced around the central opening 20 adjacent the chip 26. After wire bonding, the spaces remaining within the cavity formed by the central opening 20 are filled with an epoxy encapsulant and cured. The chip package as so formed can then be electrically tested.

In the arrangement of Fig. 7A, the apertures or stacking pockets 22 of the chip carrier 16 are spaced around the outer periphery thereof. As a result, the balls 26 protruding from the bottom surface thereof form a generally rectangular shaped ball grid array.

Fig. 7B shows an arrangement which may be used for an "end crowded" chip. The chip 26 therein is of elongated configuration and has the contacts 28 thereof at opposite ends thereof. The contacts 28 are wire bonded to the adjacent bonding pads 34 of the conductive pattern 32 at the opposite ends of the chip carrier 16. The opposite ends of the chip carrier 16 are provided with double rows of the apertures or stacking pockets 22 to provide for interconnection with the various bonding pads 32. The chip package as so formed has balls protruding from the lower surface thereof at the opposite ends of the chip package. This arrangement avoids the need to route the conductors around the corners of the chip to the sides thereof.

Like the arrangement of Fig. 7B, Fig. 7C shows an arrangement for use with an elongated chip 26 having the contacts 28 thereof at the opposite ends thereof. In the arrangement of Fig. 7C, the base layer 30 does not have the central opening 44 therein, but instead has elongated openings 68 at the opposite ends thereof so as to expose the contacts 28 at the opposite ends of the chip 26. The conductive pattern 32, which has a desired configuration, is disposed on the upper surface of the solid base layer 30, and the contacts 28 of the chip 26 are wire bonded to bonding pads 34 at the opposite ends of the base layer 30 adjacent the openings 68 therein. The conductive pattern 32 routes the bonding pads 34 to the apertures or stacking pockets 22 which are spaced along the opposite side edges of the chip carrier 16.

Fig. 8A illustrates the manner in which the chip package shown in Fig. 7A is completed. As previously noted, the chip 26 is mounted within the central opening 20 in the chip carrier 16 such as by use of an adhesive. The contacts 28 of the chip 26 are then interconnected with the bonding pads 34 of the conductive pattern 32 by wire bonding. The central opening 20 is then filled with potting compound to encapsulate the chip 26 and thereby complete the chip package. The completed chip package may then be electrically tested. The chip carrier 16 is comprised of the base layer 30, the top layer 38, the center layer 40 and the bottom layer 42. The bottom layer 42 provides a surface on which the chip 26 is mounted with adhesive when it is placed within the central opening 20.

Fig. 8B shows the manner in which the arrangement of Fig. 7C is completed. In the arrangement of Fig. 8B, the bottom layer 42 is omitted from the chip carrier 16 so that the chip 26 can be inserted through the central opening 50 in the center layer 40 for mounting at the underside of the base layer 30. The chip 26 is mounted on the underside of the base layer 30, such as by use of adhesive. The contacts 28 at the opposite ends of the chip 28 are then coupled through the apertures 68 in the base layer 30 to the bonding pads 34 of the conductive pattern 32, such as by wire bonding. The central opening 20 is then filled with potting compound. In this fashion, the chip package is completed, and may then be electrically tested. The bottom layer 42 of the chip carrier 16 is not

necessary, but may be mounted on the underside of the chip 26 opposite the base layer 30, if desired.

Figs. 9A and 9B show arrangements used in the formation of chip packages which use either chip scale packages (CSPs) or ball grid array (BGA) chips. In the case of both CSP chips and BGA chips, as opposed to the bare chips previously described, a plurality of balls or bumps are provided at a surface of the chip to define the contacts of the chip. In the arrangements of Figs. 9A and 9B, the chip carrier 16 is provided in two different pieces. A first such piece is formed by mounting the top layer 38 on the base layer 30. The base layer 30 is a continuous piece which does not have the central opening 44 therein in the manner of the previously described embodiments. The chip 26 is mounted on the underside of the base layer 30. As shown in Fig. 9A, an upper surface of the chip 26 has a plurality of bumps or balls 70 which protrude therefrom and form the contacts of the chip 26. The chip 26 may be of either the CSP or the BGA type. Both types of chips have the balls 70 on a surface thereof.

Fig. 9B is an exploded view of the arrangement of Fig. 9A, with the various portions thereof being inverted. As shown in Fig. 9B, the underside of the base layer 30 is provided with the conductive pattern 32 having bonding pads 34 located so that they are contacted by the balls 70 of the chip 26 when the chip 26 is mounted on the base layer 30. The conductive pattern 32 couples the bonding pads 34 to the apertures 22. The chip 26 is mounted on the underside of the base layer 30, such as by applying solder paste or conductive epoxy to the conductive pattern 32, placing the chip 26 in position thereon, and then reflowing the solder or curing the epoxy. The center layer 40, which forms a second part of the chip carrier 16, has adhesive applied thereto before being applied to the base layer 30. With the center layer 40 so mounted, the space defined thereby which surrounds the chip 26 is filled with potting compound to encapsulate the chip 26. The bottom layer 42 of the chip carrier 16, which is optional, can then be bonded to the underside of the chip package.

Fig. 10A is a sectional view of a stack comprised of chip packages made in accordance with the arrangement of Figs. 9A and 9B. In the case of each chip package,

the chip 26 is mounted at the underside of the base layer 30, and is encapsulated with the potting compound 18. The chip 26 is of the CSP type, and is therefore relatively thin. As shown in Fig. 10A, the total thickness of each chip package is not substantially greater than the thickness of the CSP chip therein.

Fig. 10B is similar to Fig. 10A but depicts a single chip package in which a chip 26 of the BGA type is mounted. The BGA type chip of Fig. 10 is substantially thicker than the CSP chip shown in Fig. 10A. Again, however, the total thickness of the chip package is not substantially greater than the thickness of the BGA type chip 26. Because of the greater thickness of the chip package shown in Fig. 10B, each of the apertures 22 is provided with two of the balls 24. In this manner, the lower second ball 24 protrudes outwardly from the lower surface of the chip package.

Occasionally, it may be necessary to reroute the connections of the balls 24 of a chip package externally rather than within the chip package. In such instances a transposer board 72 can be used. Fig. 11 shows a transposer board 72 mounted at the underside of a chip package. As shown therein, the transposer board 72 has a size and shape similar to that of the chip carrier 16 of the chip package. In fact, the transposer board 72 can be assembled from a top layer 38, a base layer 30, a center layer 40 and a bottom layer 42, in the manner of the chip carrier 16. However, none of the layers 38, 30, 40 and 42 are provided with central openings therein, resulting in a solid structure throughout the transposer board 72. The base layer 30 is provided with the desired conductive pattern 32. The conductive pattern 32 is routed to as to interconnect the various apertures 22 therein in desired fashion.

As previously described, the various chip packages such as the packages 12 and 14 of the chip stack 10 are mounted together when forming a stack thereof by disposing the balls 24 within the apertures 22 in the chip packages 12 and 14. The stacking pockets formed by the apertures 22 are advantageous in a number of respects. Because the balls 24 are temporarily placed within the apertures 22 and are then mechanically and electrically coupled therein, such as by using solder or conductive epoxy, the apertures 22 define confined spaces for the solder or epoxy. This prevents the solder or epoxy from

getting on other portions of the chip packages. It tends to hold the balls 24 in place while the solder is reflowed or the epoxy is heated. When the balls 24 are placed in the stacking pockets defined by the apertures 22, they are held captive in the pockets, and they are self-aligning as a stack of the chip packages is formed.

The balls 24 can be standard, commercially available metallic balls. Available balls range in size from 10 mils diameter to 35 mils diameter. 20 mil diameter balls have been used in some of the embodiments described herein. Such balls are typically made of 90% lead and 10% tin, and may be copper plated.

Alternatively, fuzz buttons can be used in place of the balls 24. Such an arrangement is shown in Figs. 12A and 12B. Fig. 12A is an exploded perspective view of a chip carrier 74. The chip carrier 74 is like the chip carrier 16 of Fig. 5, except for the bottom layer 42. In the chip carrier 74 of Fig. 12A, fuzz buttons 76 are mounted within the apertures 54 in the bottom layer 42. The fuzz buttons 76, which are generally spherical balls of conductive wire, are commercially available conductive elements.

With the fuzz buttons 76 imbedded in the apertures 54 in the bottom layer 42, the bottom layer 42 becomes a button board. The bottom layer 42 or button board may be separate from the rest of the chip carrier 74, inasmuch as its only function is to hold the fuzz buttons 76 in place. When assembling a plurality of the chip carrier 74 containing the fuzz buttons 76, a slight pressure must be applied to the stack at all times to maintain electrical contact of the fuzz buttons 76 with the conductive pattern 32 within the apertures 22. The fuzz buttons 76 are used primarily for testing of the chip packages, and are not normally permanently mounted within the apertures 22. They are used to maintain contact with the conductive patterns 32 within the apertures 22 during assembly of a stack of the chip packages for testing purposes. After testing, the stack is disassembled, following which more permanent conductive elements such as the balls 24 are mounted in the apertures 22, where they are secured by solder or conductive epoxy in the manner previously described.

Fig. 13 provides an example of a chip package using a conventional chip with the contacts thereof concentrated at the opposite ends thereof. The chip is 0.241" wide and

0.544" long. The chip is mounted in a chip carrier similar to that shown and previously described in connection with Fig. 7B. The completed chip package measures 0.320" wide by 0.740" long by 0.030" thick. The 0.030" thickness includes the protruding portions of the balls 24 extending from one surface of the chip carrier 16. A stack formed by four such chip packages has a thickness or height of 0.096", which includes the portions of the balls 24 extending from the bottom thereof.

Figs. 14A and 14B show the same chip used in the arrangement of Fig. 13, but mounted in a chip carrier of the type shown in Fig. 7C. The resulting arrangement requires 14% less mounting area than does the arrangement of Fig. 7C, but is more complex to fabricate because of the extensive conductive pattern 32. The completed chip package measures 0.330" wide by 0.620" long. As in the case of Fig. 13, the thickness of the chip package is approximately 0.030", including the portions of the balls extending from the lower surface thereof.

Fig. 15 is a sectional view of an Intel 28F640J5 "Strataflash Memory" package 80, which is in a BGA configuration. The memory package 80 includes a die 82 having bond pads 84 and an elastomer 86 at the underside thereof. A solder mask 88 is attached to the elastomer 86 by polyimide tape 90. Solder balls 92 extend downwardly through the solder mask 88, from the elastomer 86. The Intel memory package 80 of Fig. 15 has a width of 302 mils, a length of 643 mils and a height of 36 ± 2 mils which includes the solder balls 92. The solder balls 92 are spaced on a 30 mil pitch.

Figs. 16A and 16B show the memory package 80 mounted within a stackable chip carrier 94. As shown in Fig. 16B, the stackable chip carrier 94 has a continuous base layer 30 mounted on and extending over a center layer 40 having a central opening 44 therein. The memory package 80 as shown in Fig. 15 is inverted and is mounted within the central opening 44 so that the solder balls 92 thereof contact a conductive pattern 32 at the underside of the base layer 30. The conductive pattern 32, which is illustrated in Fig. 16A, includes a pattern of bonding pads 96 at a central portion thereof. The bonding pads 96 are arranged to receive individual ones of the solder balls 92 of the memory package 80, when the memory package 80 is mounted within the central opening 44 in

the center layer 40 of the stackable chip carrier 94. The conductive pattern 32 couples the bonding pads 96 to individual ones of the apertures 22 in the center layer 40. Balls 24 are mounted in the apertures 22, in the manner previously described. Because of the substantial thickness of the memory package 80, each of the apertures 22 is provided with a pair of the balls 24, as shown in Fig. 16B.

The memory package 80, the dimensions of which were previously noted, is mounted within the stackable chip carrier 94, to form a chip package measuring 400 mils wide, 760 mils long and 47 mils high or thick, including the portions of the balls 24 which extend from the underside of the chip package. The pitch of the balls 24, mounted within the apertures 22 around the periphery of the center layer 40 of the stackable chip carrier 94, is 40 mils, using balls 24 which are 20 mils in diameter. The conductive pattern 32 is etched copper foil on a 5 mil thick Kapton or equivalent plastic layer.

The chip package of Fig. 16A and 16B illustrates that BGA type dies and packages can be adapted to the stacking format, in accordance with the invention. However, because of the nature of the BGA packages, the thickness of the resulting chip package is considerably greater than in the case of chip packages using bare dies.

Chip packages and stacks according to the invention lend themselves to manufacture using a variety of techniques, many of which are conventional. For example, the three different chip carrier configurations shown in Figs. 8A, 8B, 9A and 9B can be made in strip form. Auto wire bonders designed to handle lead frames can be adapted to handle such carriers in strip format. Where chips of the CSP or BGA type must be soldered in place, the chip carrier is made in two different sections as previously described in connection with Figs. 9A and 9B. In that instance, the base layer 30 and the top layer 38 are made in strip form or panel form. Solder paste is stenciled onto the layer, the chips are placed in position, the solder is reflowed, and the remainder of the chip carrier, comprising the center layer 40 and where desired the bottom layer 42, is laminated to the base layer 30.

By way of summary of the description of the various embodiments above, the successive steps of methods of making stackable chip packages in accordance with the

invention are set forth in Fig. 17. In a first step 100, a chip carrier 16 having stacking pockets 22 and a conductive pattern 32 extending to the pockets 22 is provided. In a next step 102, a chip 26 is mounted in the chip carrier 16, such as by mounting within a central opening 20 in the carrier. Next, and in a step 104, the chip 26 is electrically connected to the conductive pattern 32 in the chip carrier 16. As previously described, this is accomplished by wire bonding in the case of bare chips or dyes. In the case of CSP or BGA type chips, electrical interconnection may be accomplished by disposing solder paste on the conductive pattern 32 and then reflowing the solder to solder the balls of the chips thereto. The chip 26 is then encapsulated within the chip carrier 16, in a step 106, using the potting compound 18. This forms a single layer integrated circuit element in accordance with the invention.

In a following step 108, the balls 24 or other conductive elements are mounted in the stacking pockets 22 so as to contact the conductive pattern 32. The balls 22 may be secured therein using conductive epoxy or solder. This completes the formation of the stackable chip package. The completed chip package may then be electrically tested in a following step 110.

Fig. 18 illustrates the successive steps of a method of assembling the chip packages into a stack, in accordance with the invention. In a first step 112, a plurality of the chip packages is provided. Each chip package has conductive elements such as the balls 24 protruding from a surface thereof. In a next step 114, a plurality of the stackable chip packages are assembled into a stack, such that the balls 24 or other conductive elements protruding from at least some of the chip packages extend into the stacking pockets 22 and into electrical contact with the conductive patterns 32 in adjacent ones of the chip packages. In a further step 116, the balls 24 or other conductive elements of at least some of the chip packages are bonded within the stacking pockets 22 of adjacent ones of the chip packages, such as by using solder or conductive epoxy. This completes the assembly of the chip package.

It will be appreciated by those skilled in the art that various advantages are provided by the chip stacks and method of making the same in accordance with the

invention. One advantage is that chips or dies of standard configuration can be used. Dies with special bump configurations are not required, as is true of some prior art techniques. Standard wedge bonding techniques can be used to electrically connect bare chips or dies within the chip carriers. Standard chip-on-board encapsulation materials can be used to encapsulate the chip mounted within the chip carrier. Metals spheres are suitable for stacking the formed chip packages and are readily available. The stacking pockets are ideally used with conductive epoxy or solder, as opposed to surface pads which make the use of the conductive epoxy or solder more difficult. The stacked arrays contain chip packages having a thickness of approximately 15-20 mils per chip package, which is approximately half that of the chip packages within conventional stacks. Each chip package can be electrically tested before being committed to a stack.

While the invention has been shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

1. A stackable chip carrier comprising the combination of:

a base layer having a conductive pattern on at least one surface thereof;

a top layer mounted on the base layer and having a central opening therein;

a center layer mounted on the base layer opposite the top layer and having a central opening therein; and

a plurality of stacking apertures extending through an entire thickness of the chip carrier defined by the base, top and center layers.

2. A stackable chip carrier in accordance with claim 1, wherein the top and center layers and a portion of the base layer other than the conductive pattern are made of plastic.

3. A stackable chip carrier in accordance with claim 1, wherein the base layer has a central opening therein which is generally coincident with the central opening in the center layer.

4. A stackable chip carrier in accordance with claim 3, wherein the central opening in the top layer is larger than the central opening in the base layer and exposes bonding pads at opposite sides thereof formed by the conductive pattern of the base layer.

5. A stackable chip carrier in accordance with claim 1, further including a bottom layer mounted on the center layer opposite the base layer and having apertures therein aligned with the plurality of stacking apertures.

6. A stackable chip carrier in accordance with claim 5, wherein the top, center and bottom layers and a portion of the base layer other than the conductive pattern are made of Kapton.

7. A stackable chip carrier in accordance with claim 1, wherein the base layer

has layers of copper cladding on opposite sides thereof which are etched to form a desired conductive pattern.

8. A stackable chip carrier in accordance with claim 7, wherein the base layer has an aperture therein within at least one of the stacking apertures which is plated through between the layers of copper cladding.

9. A stackable chip carrier in accordance with claim 7, wherein the base layer has the layers of copper cladding on opposite sides thereof within at least one of the stacking apertures.

10. A stackable chip carrier in accordance with claim 7, wherein the base layer has an aperture therein adjacent at least one of the stacking apertures which is plated through between the layers of copper cladding.

11. A stackable chip carrier in accordance with claim 7, wherein the base layer has an aperture therein within at least one of the stacking apertures, and one but not the other of the layers of copper cladding extends through the aperture in the base layer.

12. A stackable chip carrier in accordance with claim 7, wherein a portion of one of the layers of copper cladding extends between an adjacent pair of the stacking apertures, and the base and center layers have apertures therethrough adjacent the portion of one of the layers of copper cladding, whereby a tool can be inserted through the apertures in the base and center layers to sever the portion of one of the layers of copper cladding.

13. A stackable IC chip package comprising the combination of:

a chip carrier having a thickness between opposite surfaces, a central opening therein, a plurality of stacking apertures extending through the thickness of the carrier

between the opposite surfaces and a conductive pattern therein extending from the central opening to the plurality of apertures;

a chip mounted in and encapsulated with a sealing compound within the central opening and electrically coupled to the conductive pattern; and

a plurality of conductive elements mounted in the stacking apertures in electrical contact with the conductive pattern and protruding from at least one of the opposite surfaces of the chip carrier.

14. A stackable IC chip package in accordance with claim 13, wherein the chip carrier is made of plastic.

15. A stackable IC chip package in accordance with claim 14, wherein the chip carrier comprises a laminate of plastic layers made using a flex circuit technique.

16. A stackable IC chip package in accordance with claim 13, wherein the chip has a plurality of contacts thereon spaced around a perimeter thereof, the conductive pattern has a plurality of conductive pads spaced around the central opening in the chip carrier and wire bonded to the contacts spaced around the perimeter of the chip, and the stacking apertures are spaced around a perimeter thereof and include portions of the conductive pattern which are coupled to the conductive pads.

17. A stackable IC chip package in accordance with claim 13, wherein the chip has a plurality of contacts thereon at opposite ends thereof, the conductive pattern has a plurality of conductive pads at opposite ends of the central opening in the chip carrier and wire bonded to the contacts at the opposite ends of the chip, and the stacking apertures are located at opposite ends of the chip carrier adjacent the conductive pads.

18. A stackable IC chip package in accordance with claim 13, wherein the chip has a plurality of contacts thereon at opposite ends thereof, the chip carrier has a

layer therein adjacent the chip and with openings in opposite ends thereof adjacent the contacts at opposite ends of the chip and a conductive pattern thereon having pads adjacent the openings in the opposite ends of the layer, the pads being wire bonded to the contacts at the opposite ends of the chip, the stacking apertures being spaced along opposite sides of the chip carrier between the openings in the opposite ends of the layer and the conductive pattern on the layer extending to the stacking apertures.

19. A stackable IC chip package in accordance with claim 13, wherein the chip has a plurality of ball contacts protruding from a surface thereof which are soldered to the conductive pattern.

20. A stackable IC chip package in accordance with claim 19, wherein the plurality of ball contacts comprise a ball grid array of contacts on the surface of the chip.

21. An IC chip stack comprising the combination of:

a stack of single layer integrated circuit elements, each having a chip carrier with a chip mounted therein, a plurality of stacking apertures extending through a thickness of the chip carrier between opposite surfaces thereof and a conductive pattern within the chip carrier electrically coupled to the chip and extending to the stacking apertures; and

a plurality of conductive elements disposed between adjacent pairs of the stack of single layer integrated circuit elements and each extending into stacking apertures in the adjacent pair and into electrical contact with the conductive patterns within the chip carriers of the adjacent pair.

22. An IC chip stack in accordance with claim 21, wherein the conductive elements comprise metallic balls.

23. An IC chip stack in accordance with claim 21, wherein each of the conductive elements is mounted in the stacking apertures of the adjacent pair using

solder.

24. An IC chip stack in accordance with claim 21, wherein each of the conductive elements is mounted in the stacking apertures of the adjacent pair using conductive epoxy.

25. An IC chip stack in accordance with claim 21, further including a transposer board mounted within the stack of single layer integrated circuit elements, the transposer board having a size and shape similar to each of the single layer integrated circuit elements, a plurality of stacking apertures extending through a thickness of the transposer board between opposite surfaces thereof and a conductive pattern within the transposer board extending to the stacking apertures and providing desired interconnections between the stacking apertures.

26. A method of assembling a stackable IC chip package, comprising the steps of:

providing a chip carrier having a thickness between opposite surfaces, a central opening therein, a plurality of apertures extending through the thickness of the carrier between the opposite surfaces, and a conductive pattern therein extending from the central opening to the plurality of apertures;

mounting a chip in the central opening of the carrier;

electrically connecting the chip to the conductive pattern in the carrier;

filling the central opening with a compound to encapsulate the chip therein and form a single layer integrated circuit element; and

mounting a plurality of conductive elements in the apertures of the chip carrier so that the elements make electrical contact with the conductive pattern in the carrier and form a plurality of conductive columns in the chip carrier.

27. A method in accordance with claim 26, wherein the conductive elements

protrude from at least one of the opposite surfaces of the chip carrier to facilitate physical and electrical interconnection with adjacent single layer integrated circuit elements when formed into a stack therewith.

28. A method in accordance with claim 26, wherein the conductive elements comprise metallic balls.

29. A method in accordance with claim 26, wherein the conductive elements comprise masses of wire.

30. A method in accordance with claim 26, wherein the carrier is made of plastic.

31. A method in accordance with claim 26, wherein the carrier comprises a stack of different layers which is made using a flex circuit technique.

32. A method in accordance with claim 26, comprising the further steps of:

providing a plurality of the single layer integrated circuit elements with a plurality of the conductive elements mounted in the apertures of the chip carriers thereof; and

assembling the plurality of single layer integrated circuit elements into a stack so that the conductive elements protruding from the carriers of at least some of the single layer integrated circuit elements extend into apertures and into electrical contact with the conductive pattern therein in the carriers of adjacent ones of the single layer integrated circuit elements.

33. A method in accordance with claim 26, wherein the conductive pattern includes a plurality of bonding pads at the central opening, and the step of electrically connecting the chip to the conductive pattern comprises wire bonding the chip to the plurality of bonding pads.

34. A method in accordance with claim 26, wherein a plurality of conductive elements are mounted in the apertures of the chip carrier using epoxy which is heated to cure the epoxy.

35. A method in accordance with claim 26, wherein a plurality of conductive elements are mounted in the apertures of the chip carrier using solder paste which is heated to solder the conductive elements therein.

36. A method in accordance with claim 26, wherein the steps of providing a chip carrier, mounting a chip and electrically connecting, together comprise the steps of:

providing a first portion of a chip carrier having a plurality of apertures extending therethrough and a conductive pattern disposed on a surface thereof and extending to the plurality of apertures;

mounting a chip on the surface of the first portion of a chip carrier so as to electrically couple the chip to the conductive pattern disposed on the surface;

providing a second portion of a chip carrier having a central opening therein and a plurality of apertures extending therethrough; and

mounting the second portion of a chip carrier on the first portion of a chip carrier so that the central opening of the second portion surrounds the chip and the holes therethrough are aligned with the holes in the first portion of a chip carrier.

37. A method in accordance with claim 36, wherein the chip has a plurality of ball contacts protruding from a surface thereof and the step of mounting a chip includes the steps of applying solder paste to the conductive pattern, placing the ball contacts of the chip in contact with the conductive pattern and reflowing the solder paste to solder the ball contacts to the conductive pattern.

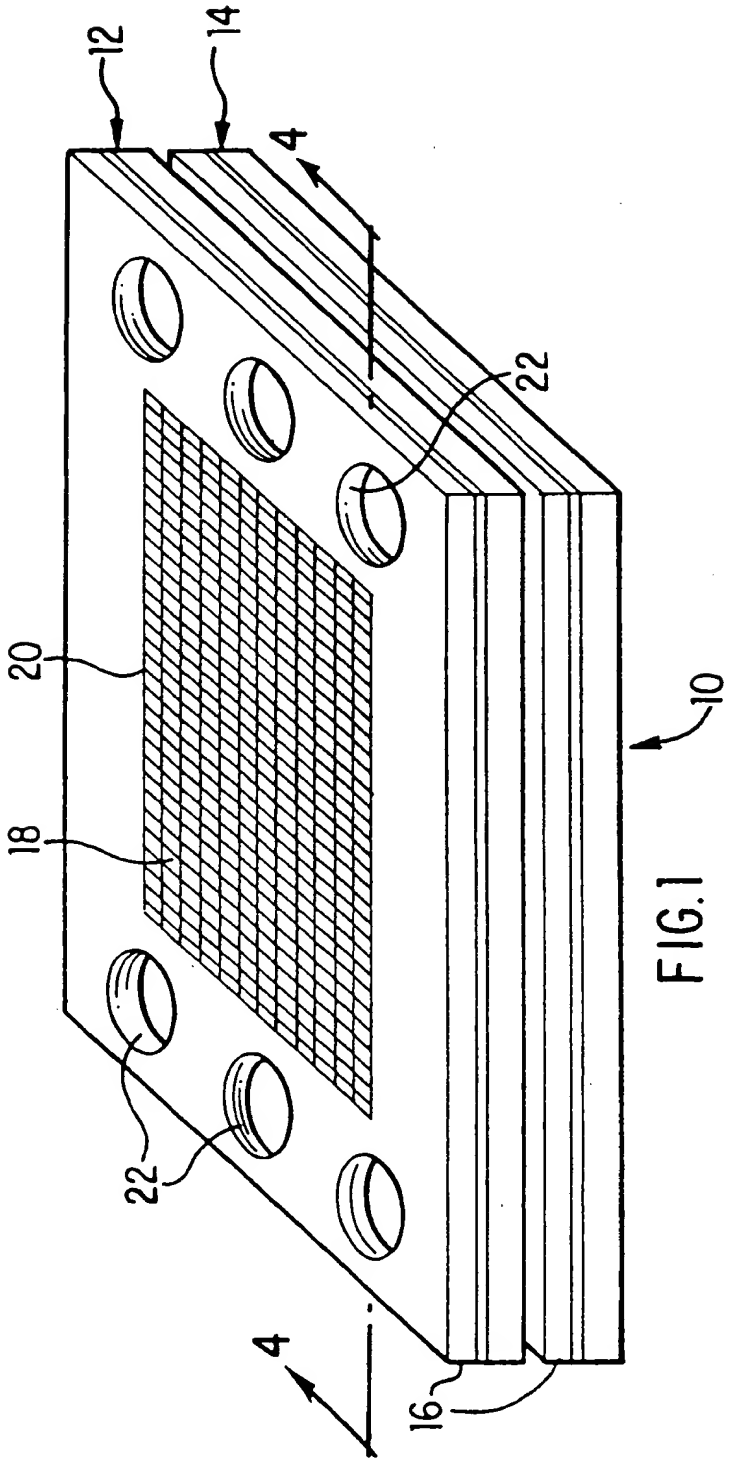

FIG.1

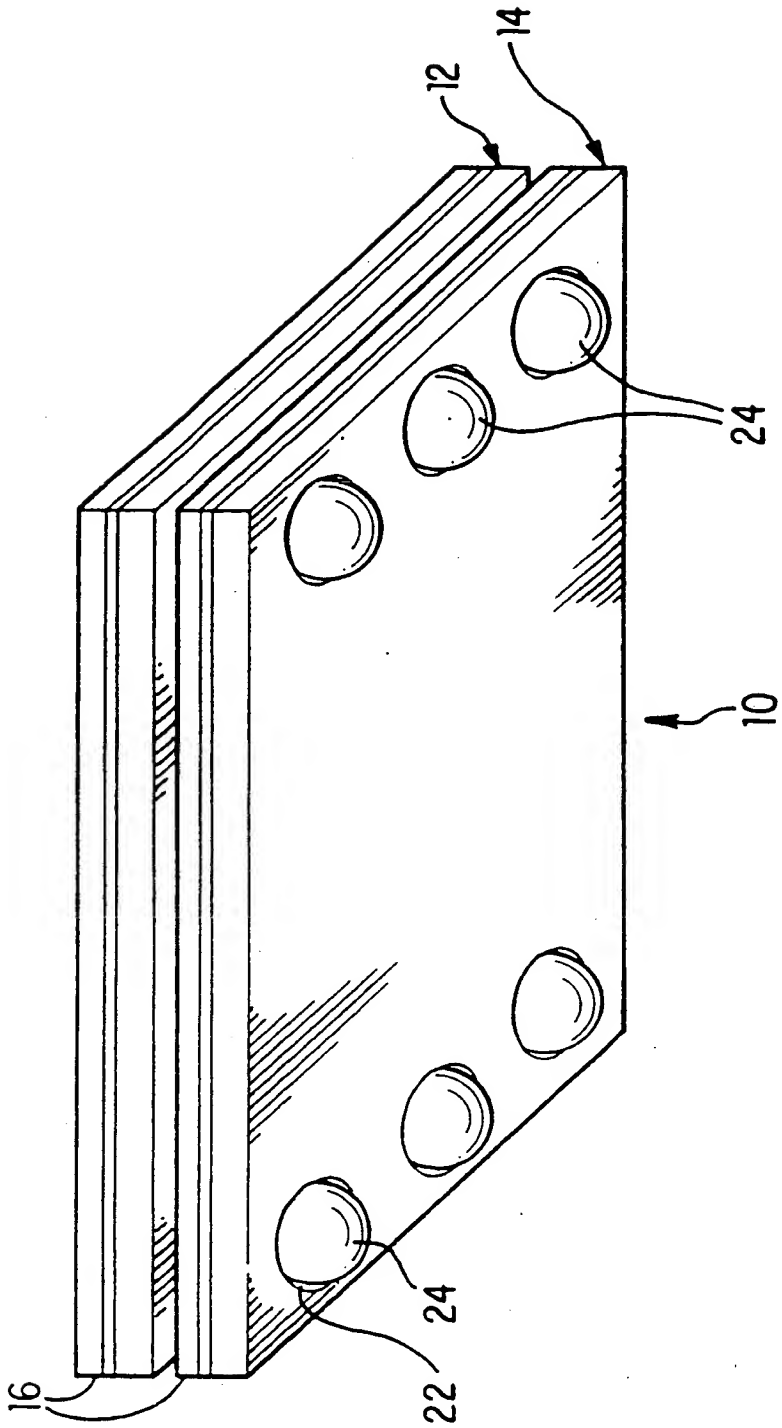

FIG.2

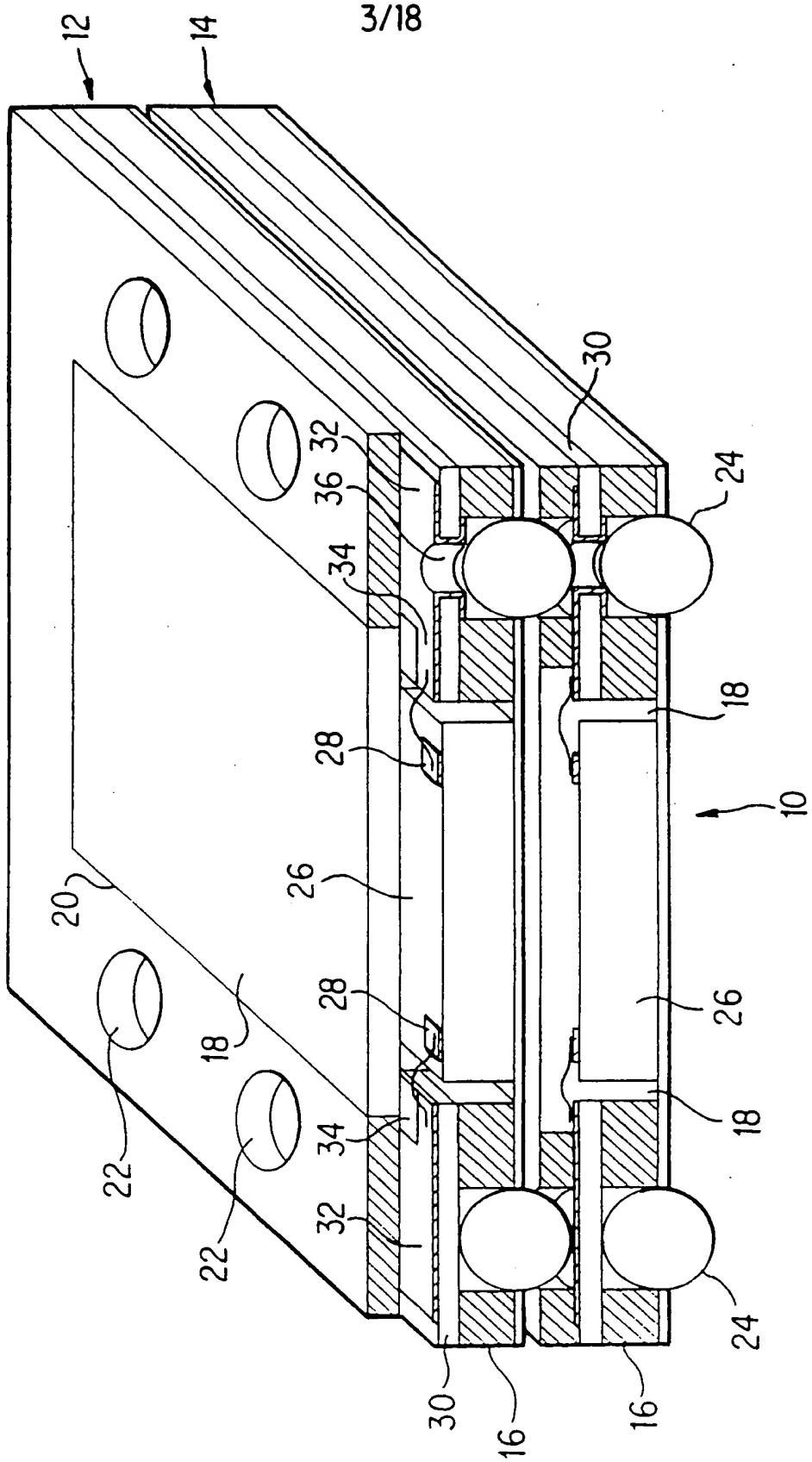

FIG. 3

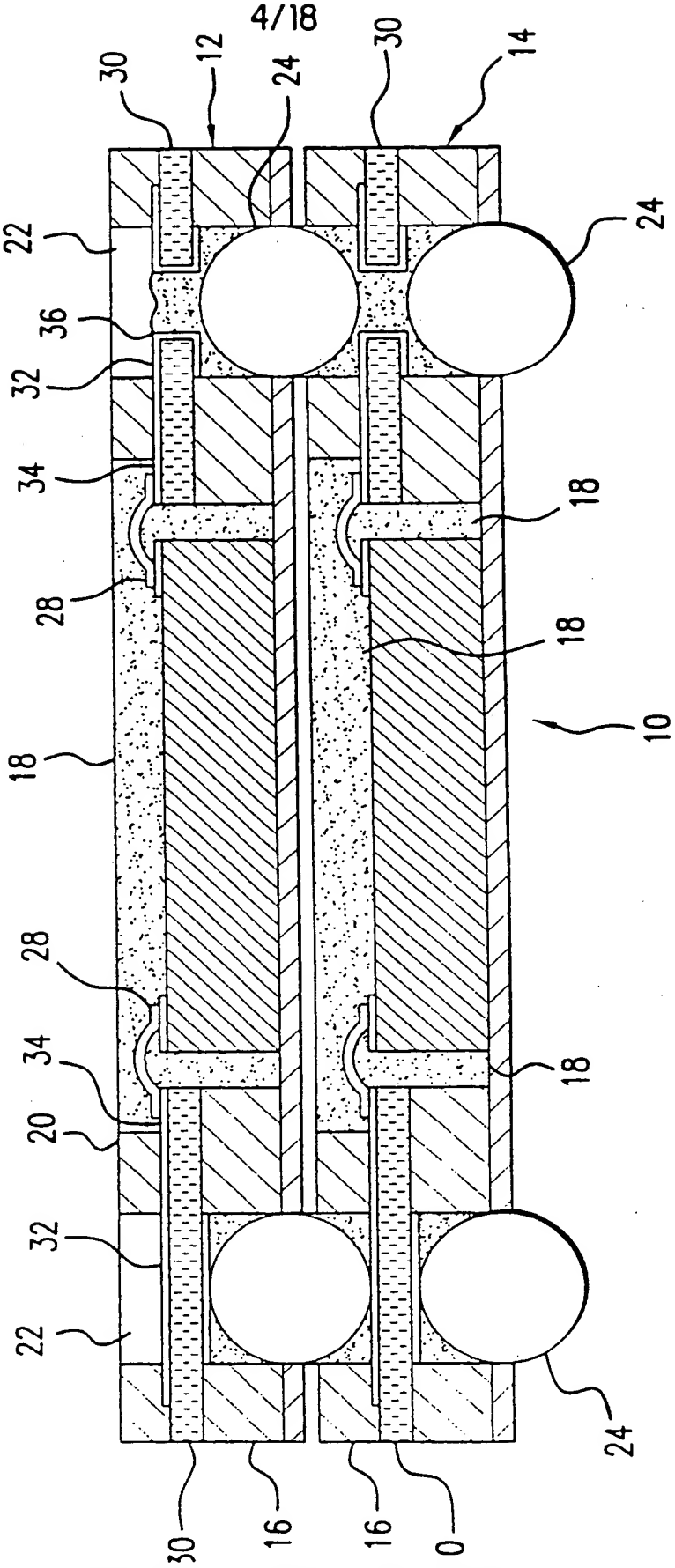

FIG.4

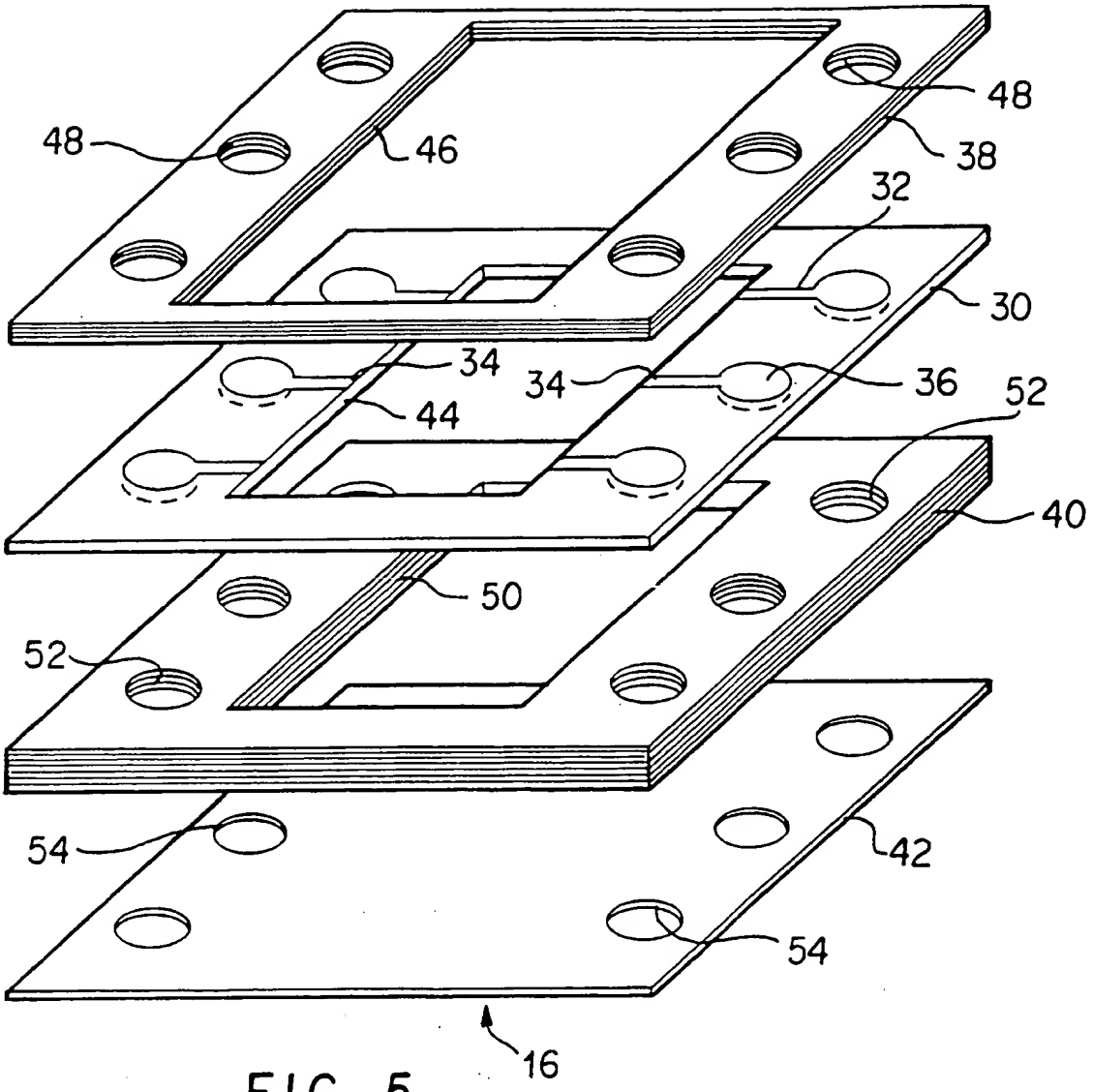

FIG. 5

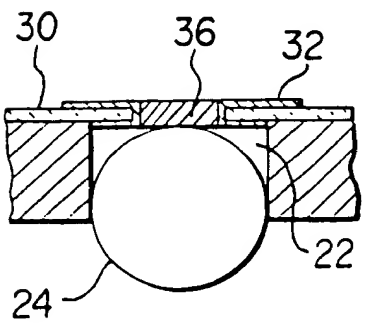

FIG. 6A

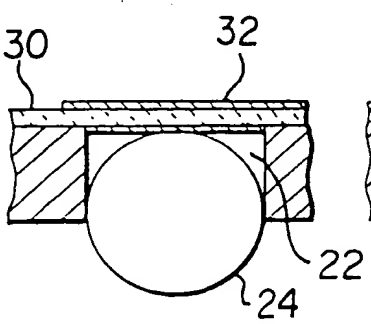

FIG. 6B

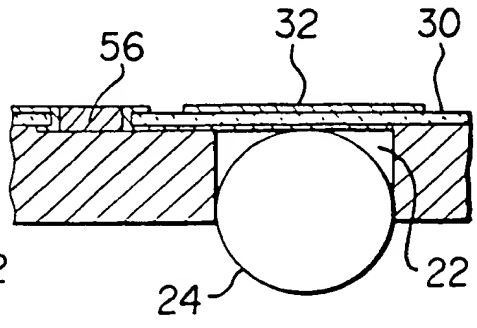

FIG. 6C

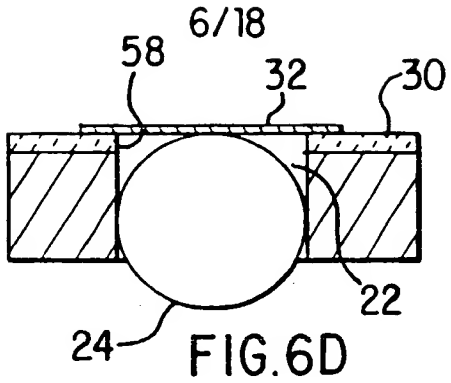

FIG.6D

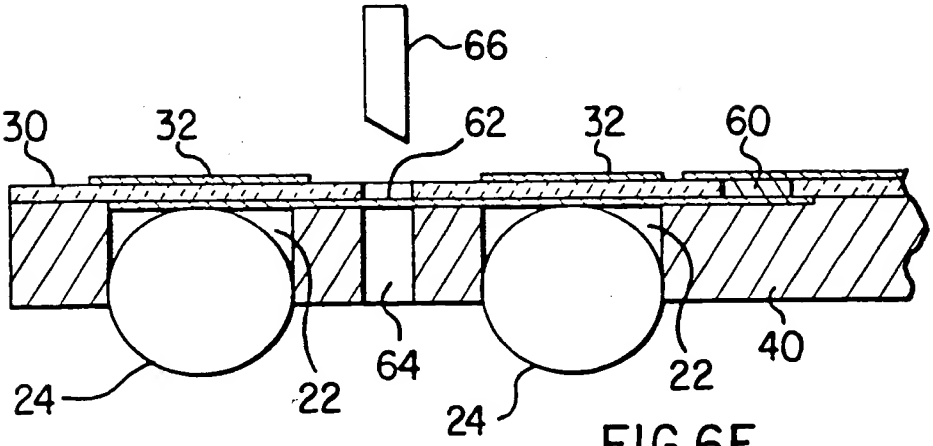

FIG.6E

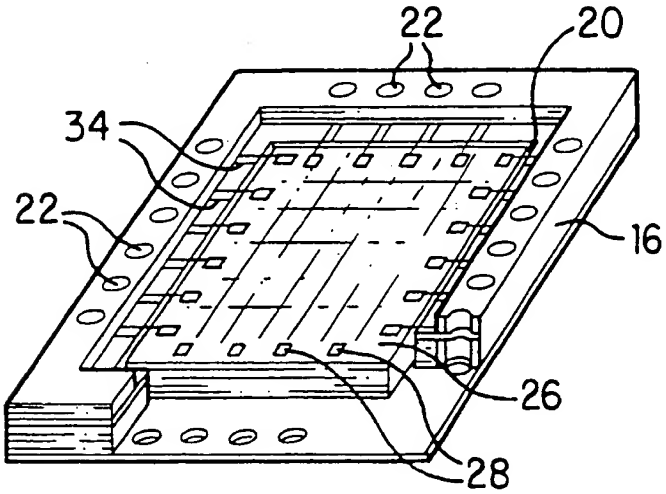

FIG.7A

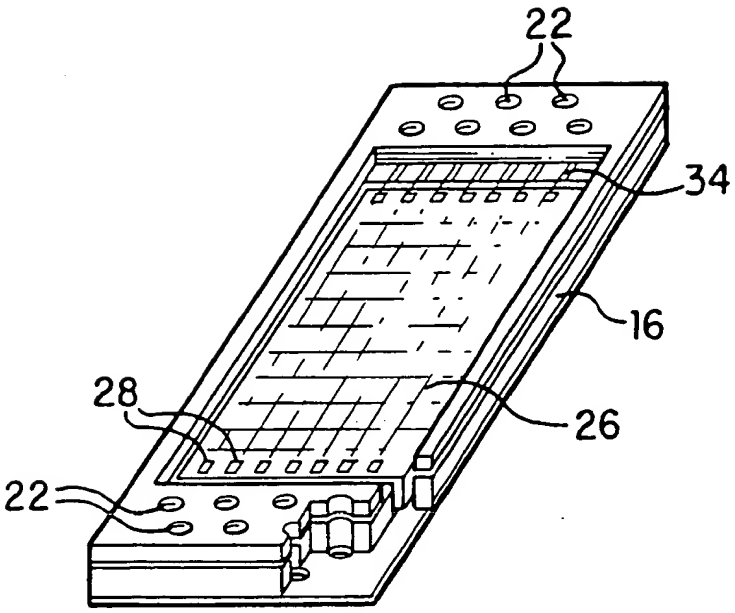

FIG.7B

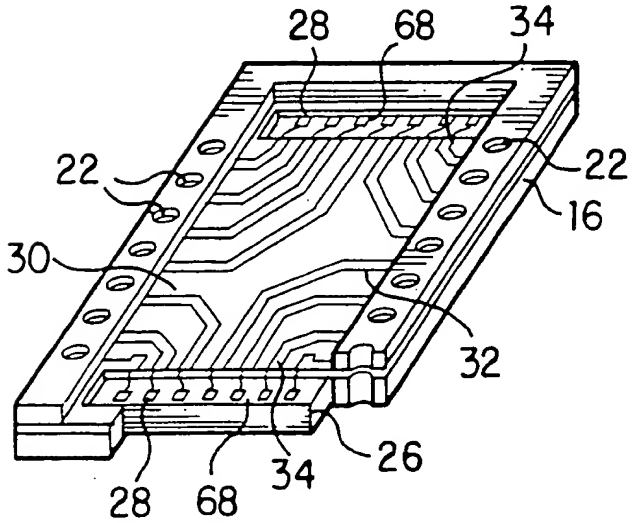

FIG.7C

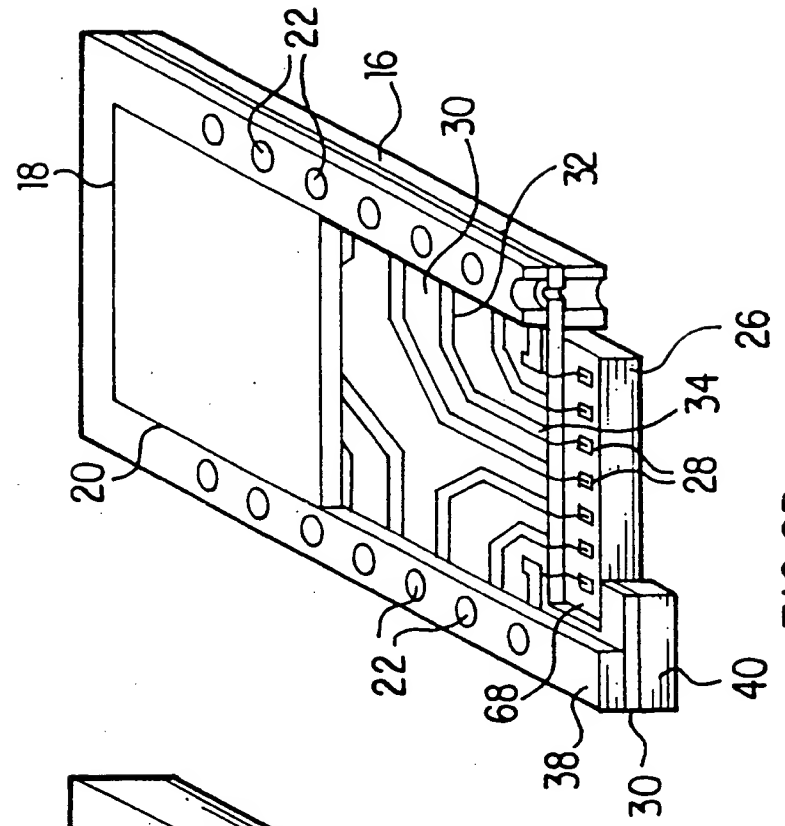

FIG.8B

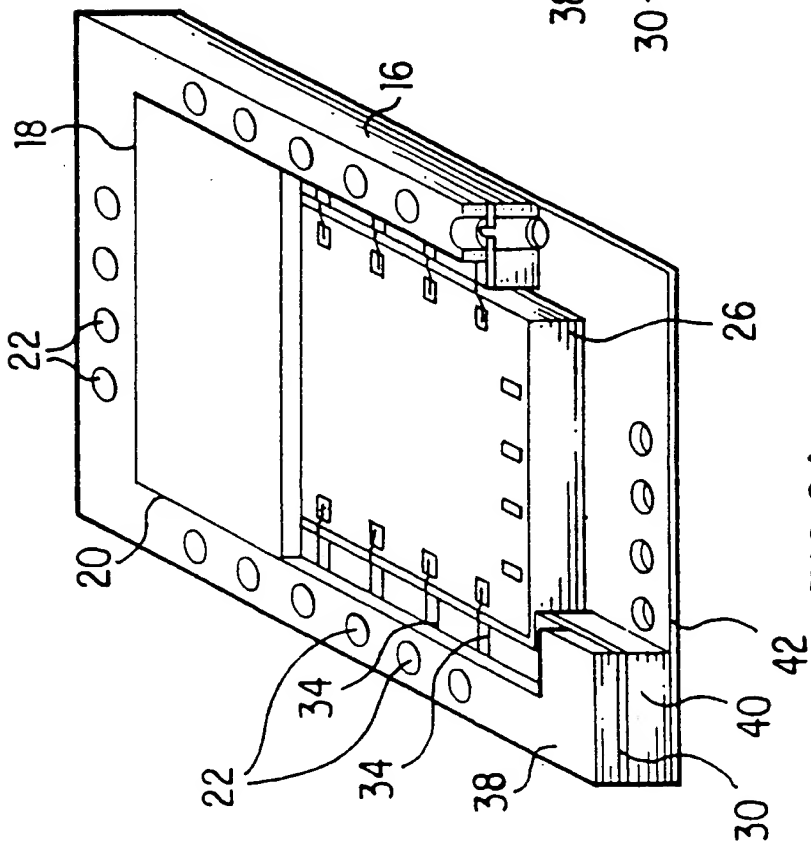

FIG.8A

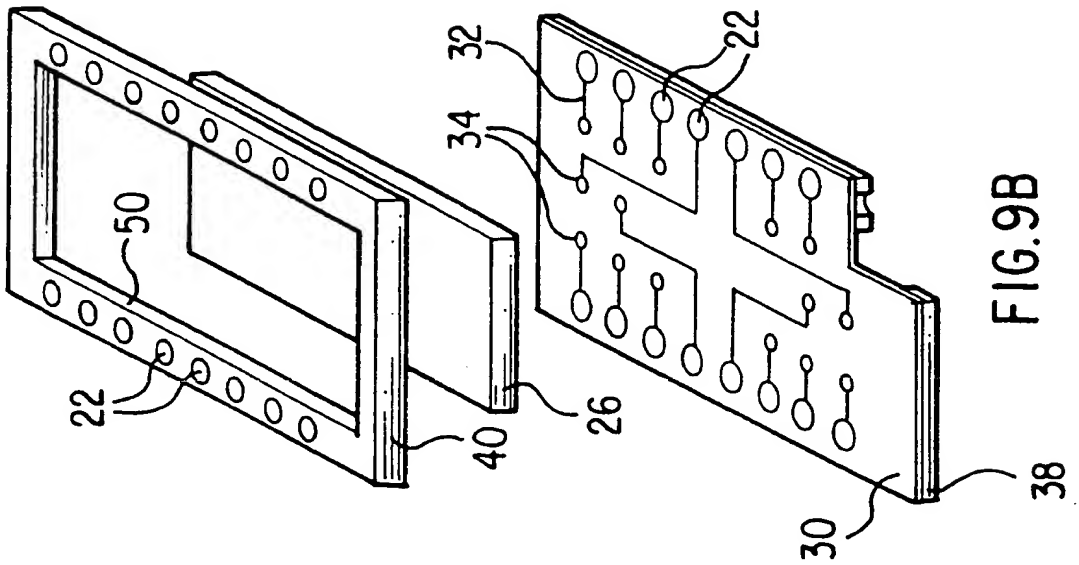

FIG.9B

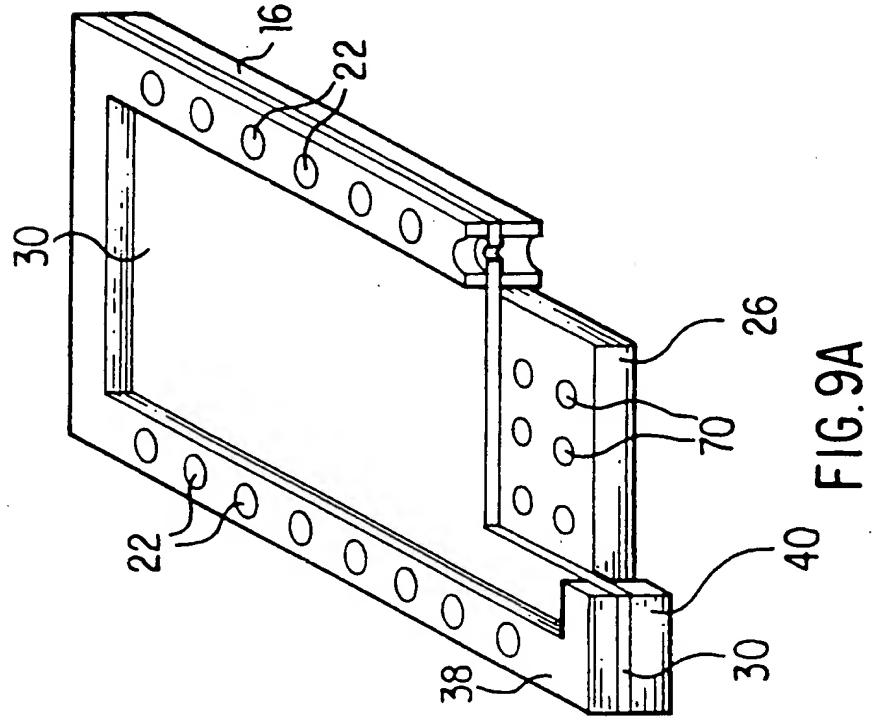

FIG.9A

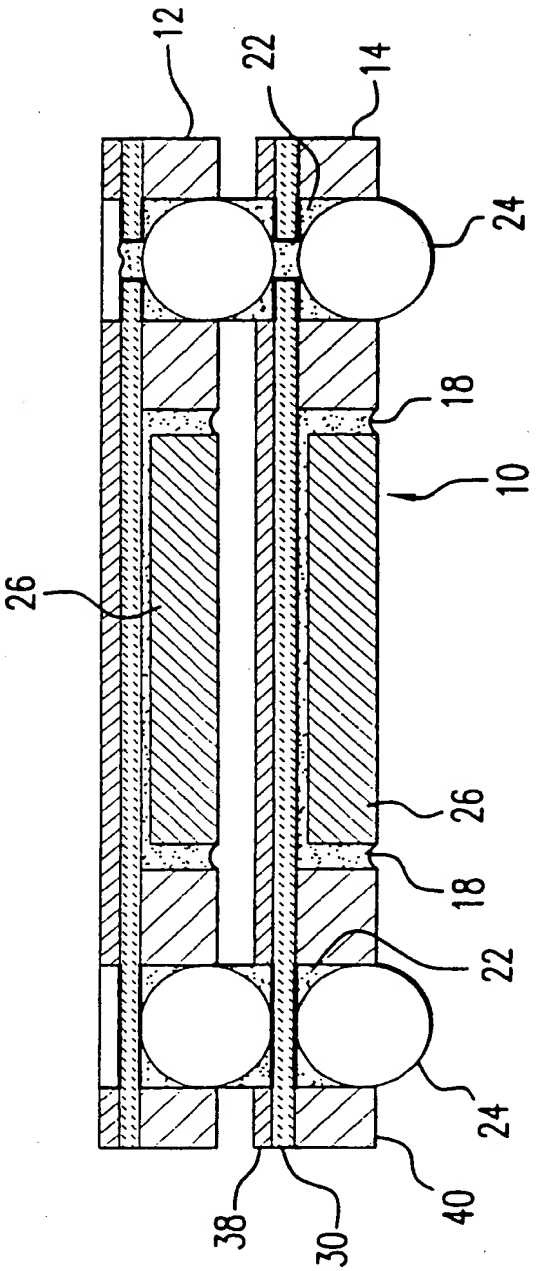

FIG.10A

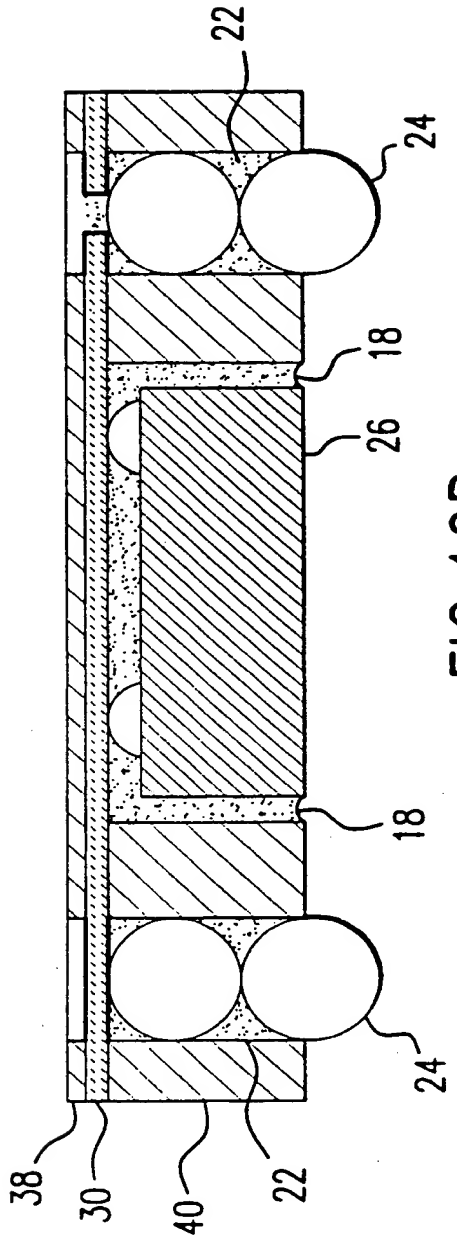

FIG.10B

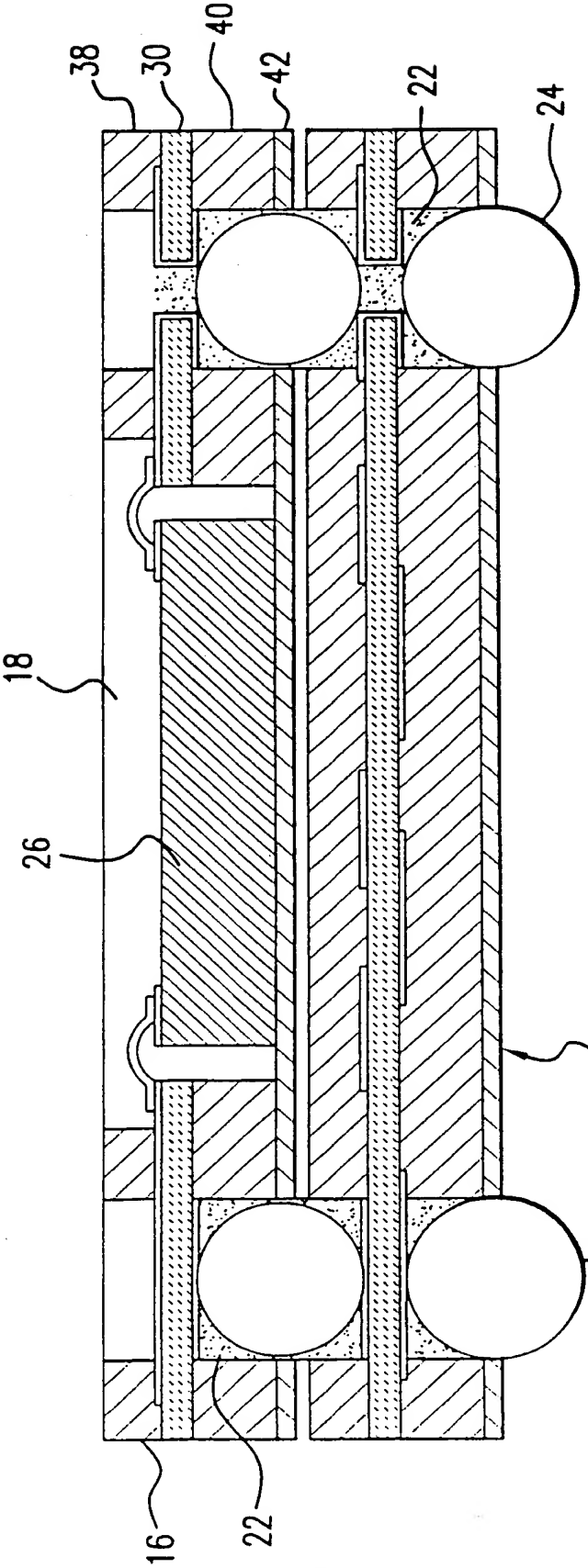

FIG.11

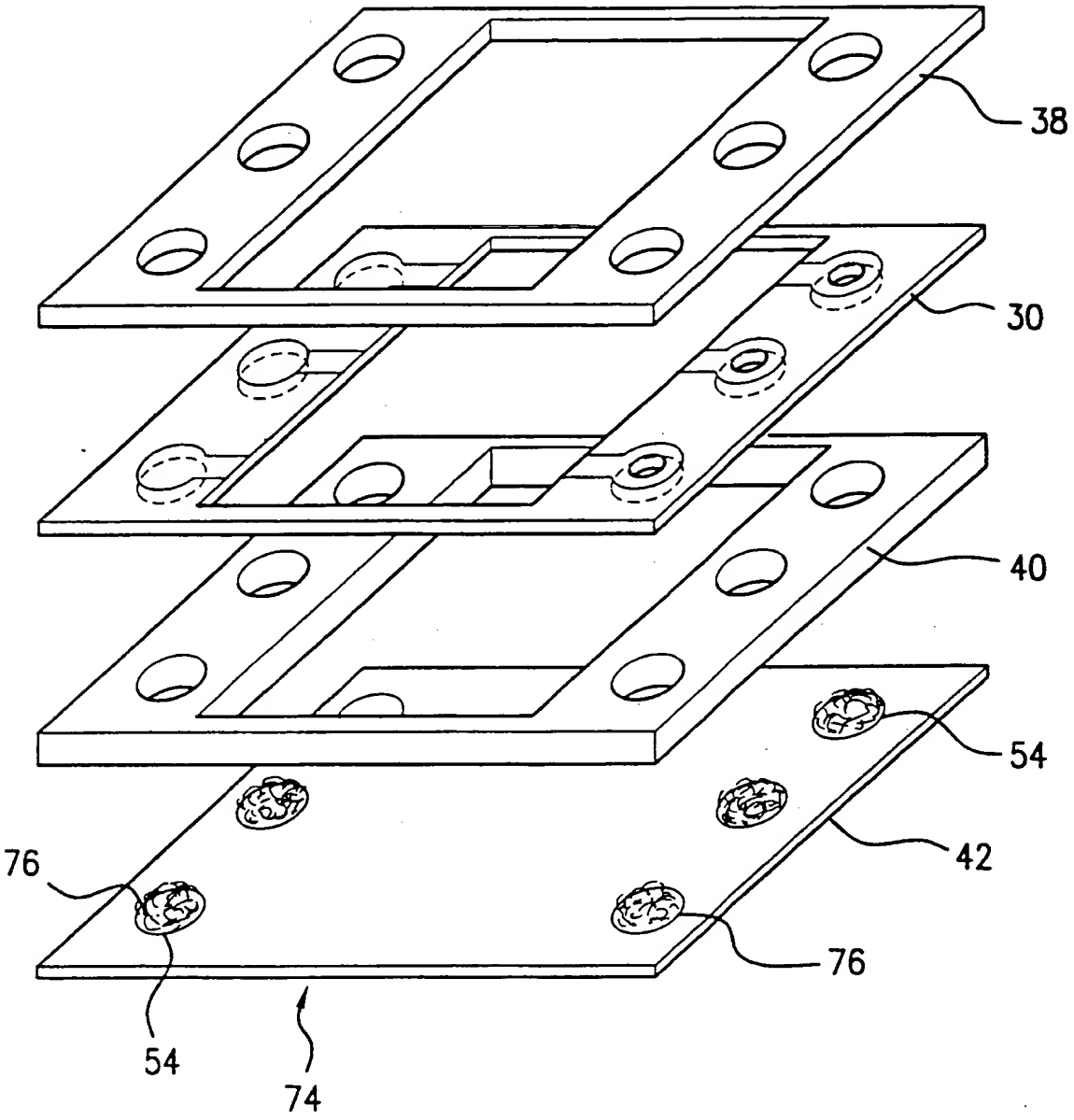

FIG. 12A

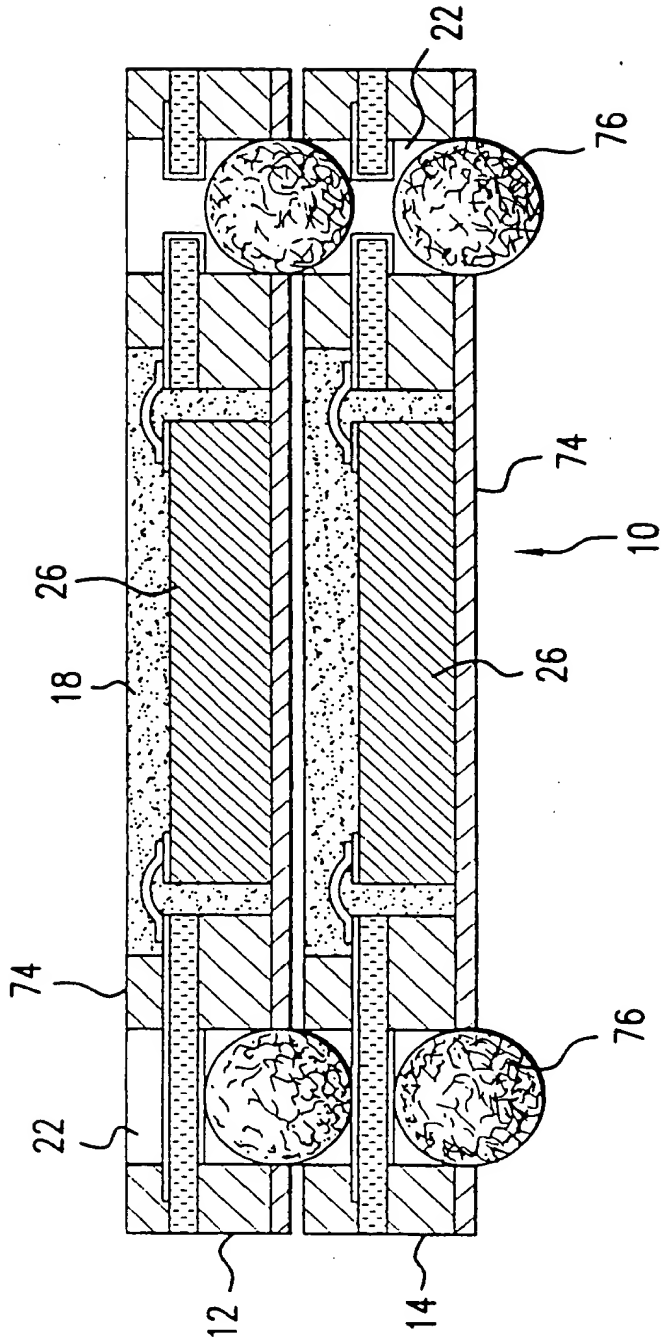

FIG.12B

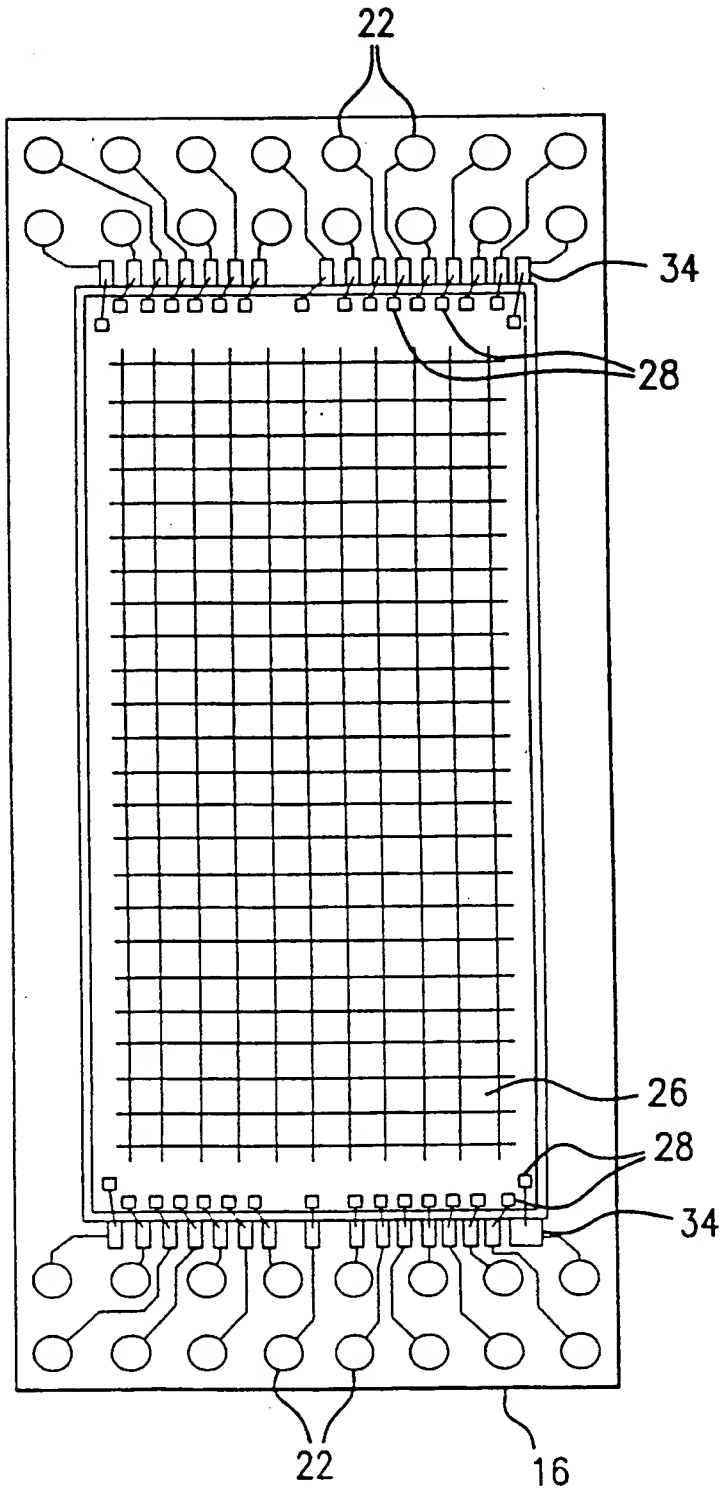

FIG.13

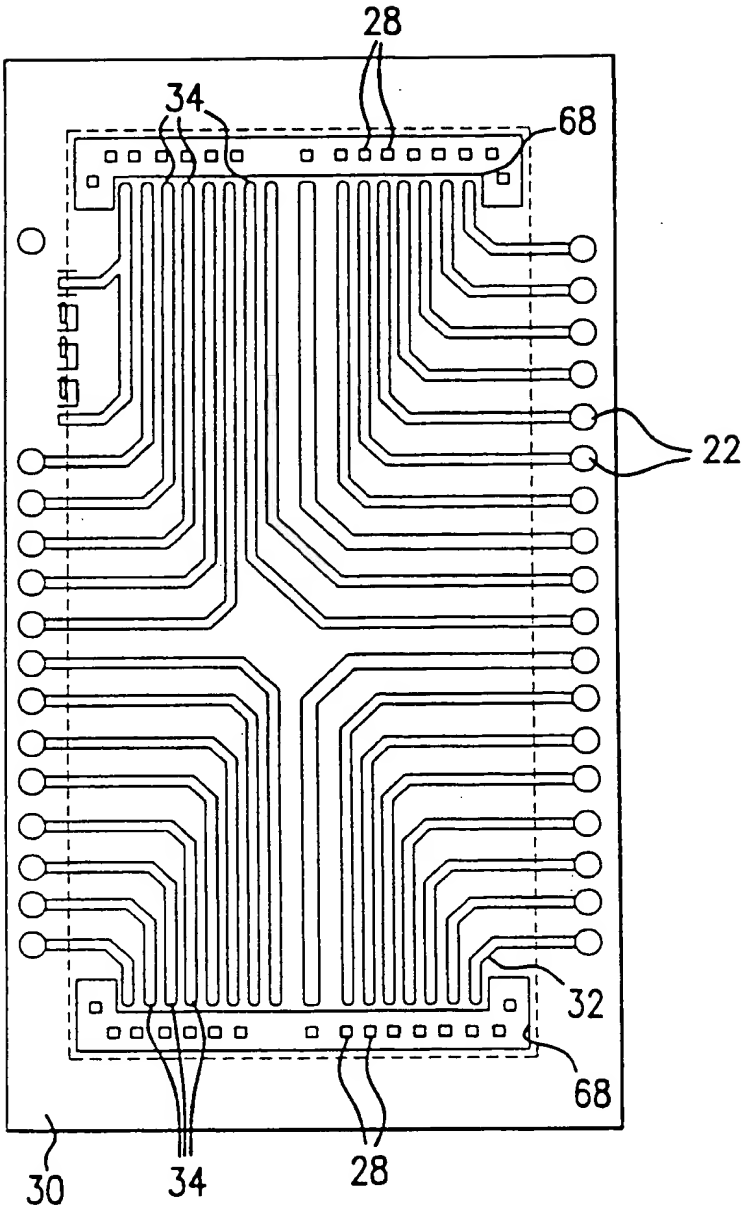

FIG.14A

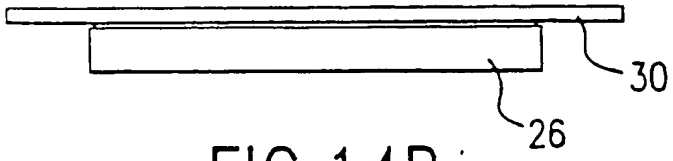

FIG.14B

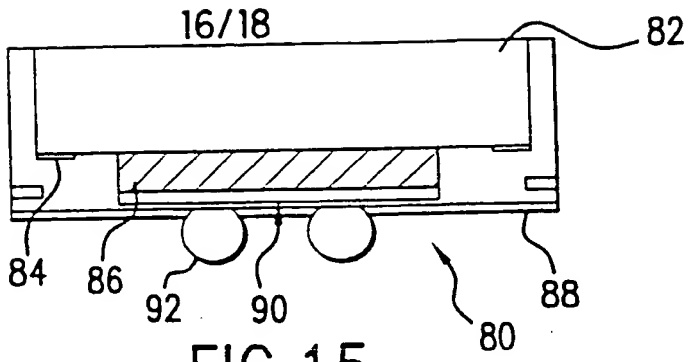

FIG.15

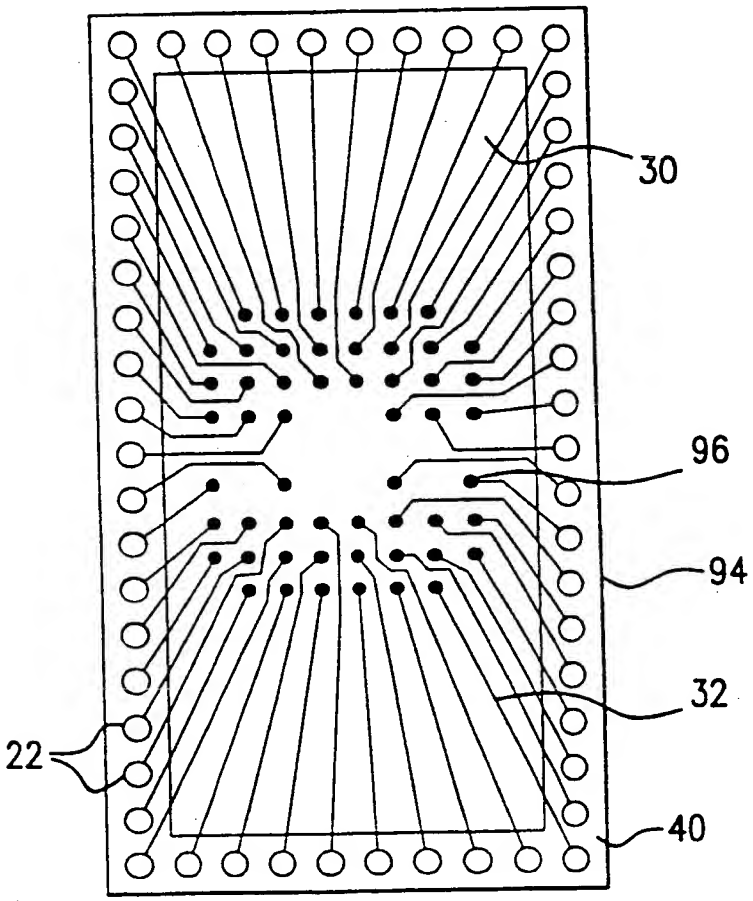

FIG.16A

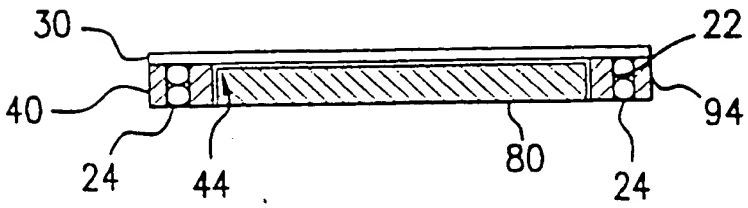

FIG.16B

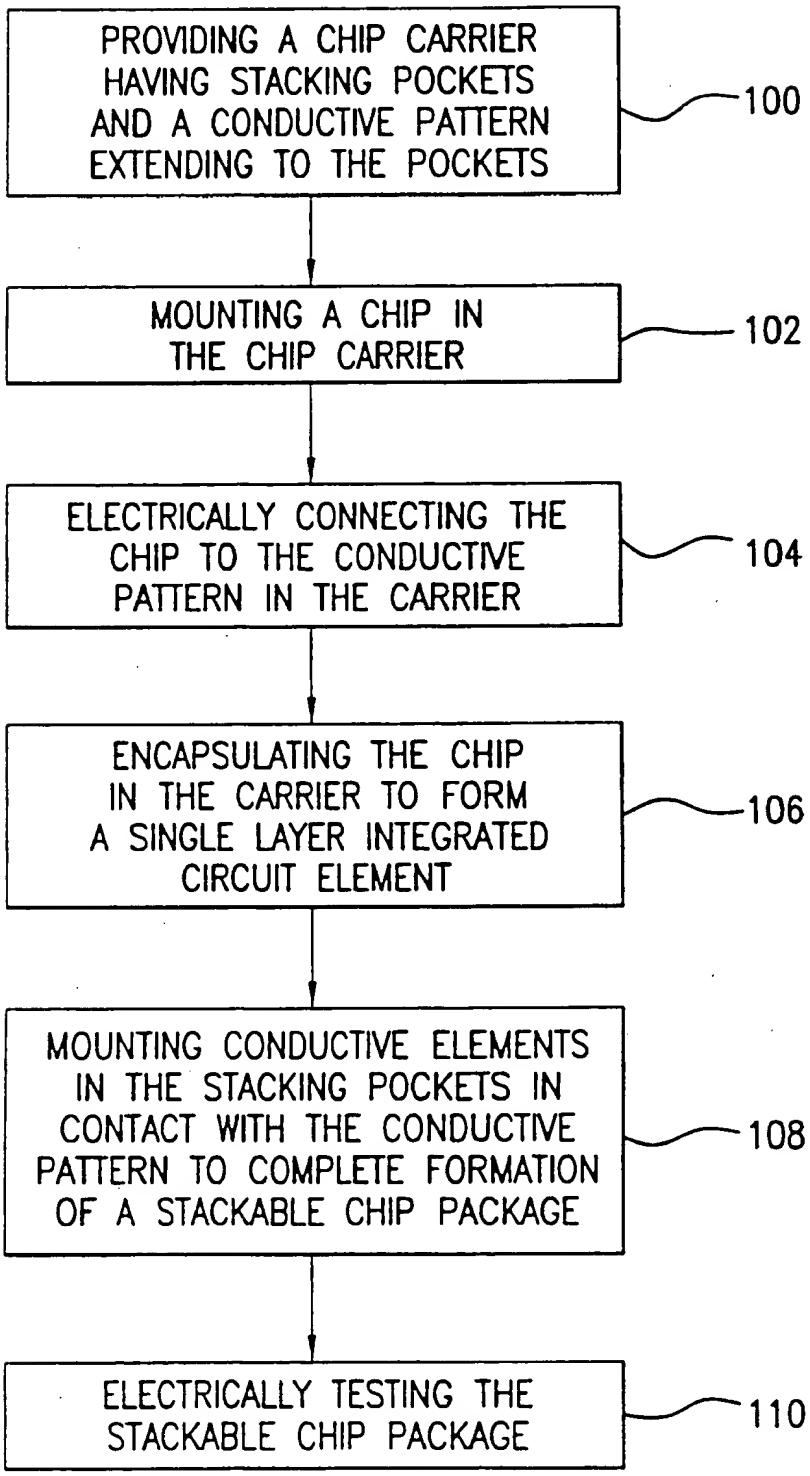

FIG.17

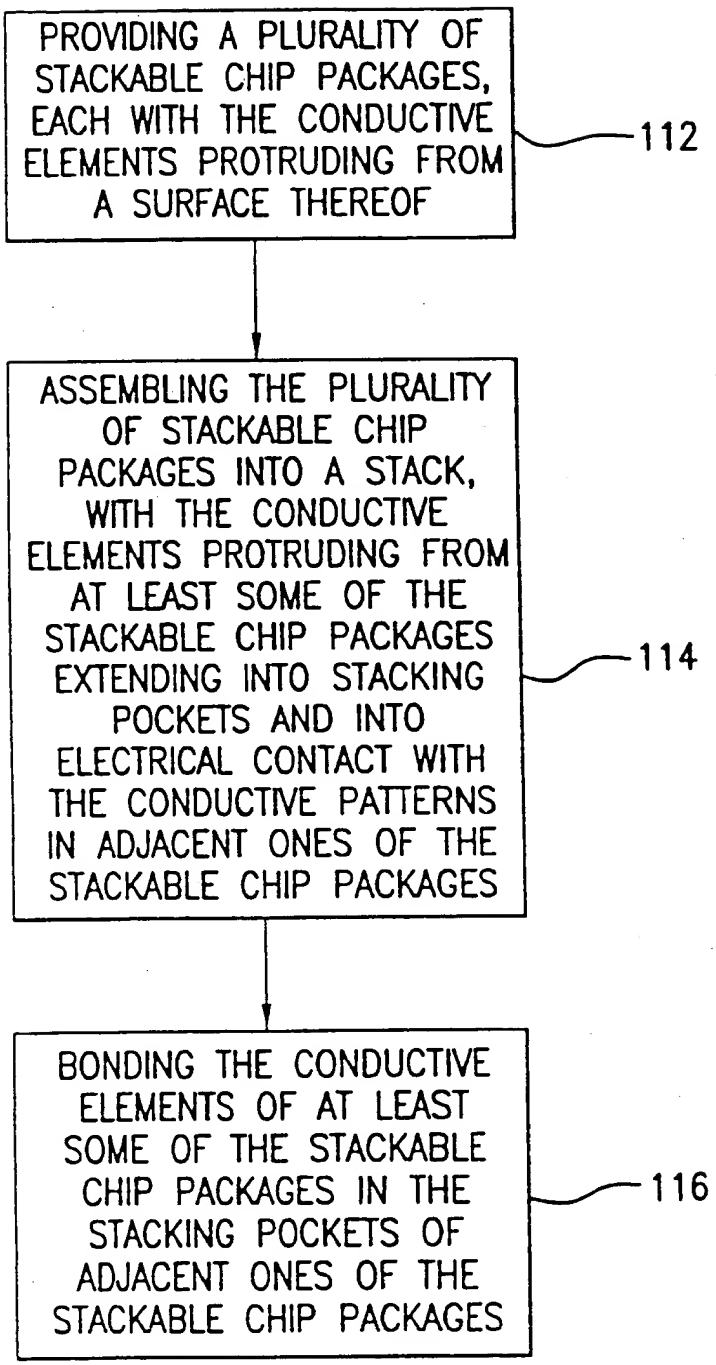

FIG.18

INTERNATIONAL SEARCH REPORT

In ational Application No
PCT/US 99/09744

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L25/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 97 11492 A (HITACHI LTD ;SASAKI YASUHIKO (JP); KOHNO AKIOMI (JP); HORINO MASAY) 27 March 1997 see abstract; figures 1,2,6	1-3, 5-11, 13-15, 19-21, 26,27, 30-32, 34,36
A	US 5 440 171 A (MIYANO ICHIRO ET AL) 8 August 1995 see the whole document	1-3, 5-11, 13-15, 19-21, 26,27, 30-32,36

-/--

[X] Further documents are listed in the continuation of box C

[X] Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search	Date of mailing of the international search report
1 July 1999	08/07/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Prohaska, G

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INTERNATIONAL SEARCH REPORT

Ir. ational Application No
PCT/US 99/09744

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 729 184 A (NIPPON ELECTRIC CO) 28 August 1996 see abstract; figures	4,16-18, 22-24, 28, 33-35,37
A	EP 0 479 205 A (NORTON CO) 8 April 1992 see abstract; figures 1,3-8,12,14	4,16-18, 25,33
A	EP 0 759 637 A (NIPPON ELECTRIC CO) 26 February 1997 see abstract; figures 3-14	29

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

In. ational Application No
PCT/US 99/09744

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Form PCT/ISA/210 (patent family annex) (July 1992)